CMOS IC of Real Time Watch with Serial Interface, 56 X 8 RAM

Microcircuit HT1307A is essentially the binary – decimal digital watch with a calendar, it has the additional 56 bytes of the power self-sufficient static RAM and possesses the low power consumption. The addresses and data are applied consecutively via the two-wire bi-directional bus. The microcircuit is intended for count of the real time in hours, minutes and seconds, count of week days, date, month and year. The last day of the month is automatically adjusted for the months of less, than 31 days, including correction for the leap year. The watches function in the 24-hour format or in the 12-hour format with the AM / PM-indicator. Microcircuit HT1307A has the built-in power supply control circuit, which determines the supply disruption and automatically switches over the device into the battery mode.

Functions and Features

- Count of seconds, minutes, hours, week days, date, months and years with consideration of the leap years (before 2100);
- 56 bytes of the power self-sufficient RAM for the data storage;
- Two-wire consecutive interface;
- Programmable rectangular output signal;
- Automatic determination of the supply voltage drop and the switching diagram;
- Consumption of less than 500 nA in the back-up supply mode with the operating generator;
- Temperature range of the industrial application: -40°C – +85°C.
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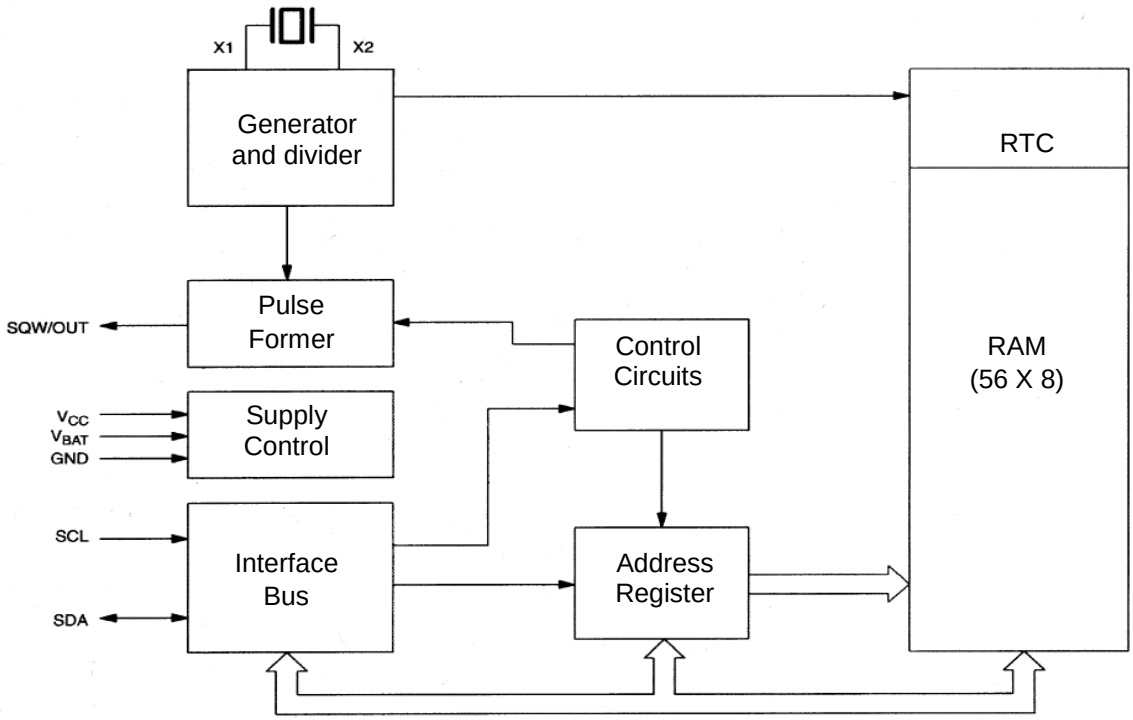
Structural Diagram HT1307A



HT1307A Operating Temperatures Range

Operating temperatures range of the microcircuit HT1307A: T_A = - 40 ... + 85 °C.

HT1307A Limit Mode

Limit and limit permissible operational modes of the microcircuit HT1307A are listed in the Table

Parameter Description, Measurement Unit	Identification	Norm			
		Limit Permissible		Limit	
		min	max	min	max
Supply voltage, V	V_{CC}	4.5	5.5	-0.5	7.0
Battery voltage, V	V_{BAT}	2.0	3.5	-0.5	7.0
Low level input voltage, V	V_{IL}	-0.3	0.8	-0.5	7.0
High level input voltage, V	V_{IH}	2.2	V_{CC}+ 0.3	-0.5	7.0
Storage temperature, °C	T_S	-	-	-55	+125

All voltages are indicated relative to ground. Under influence of the limit mode serviceability of the microcircuits is not guaranteed. After measuring the limit mode serviceability is guaranteed in the limit permissible mode.

Electric Parameters of HT1307A

Electric parameters of the microcircuit HT1307A (T_A = –40...+ 85°C, V_{CC} = 4.5 – 5.5 V)

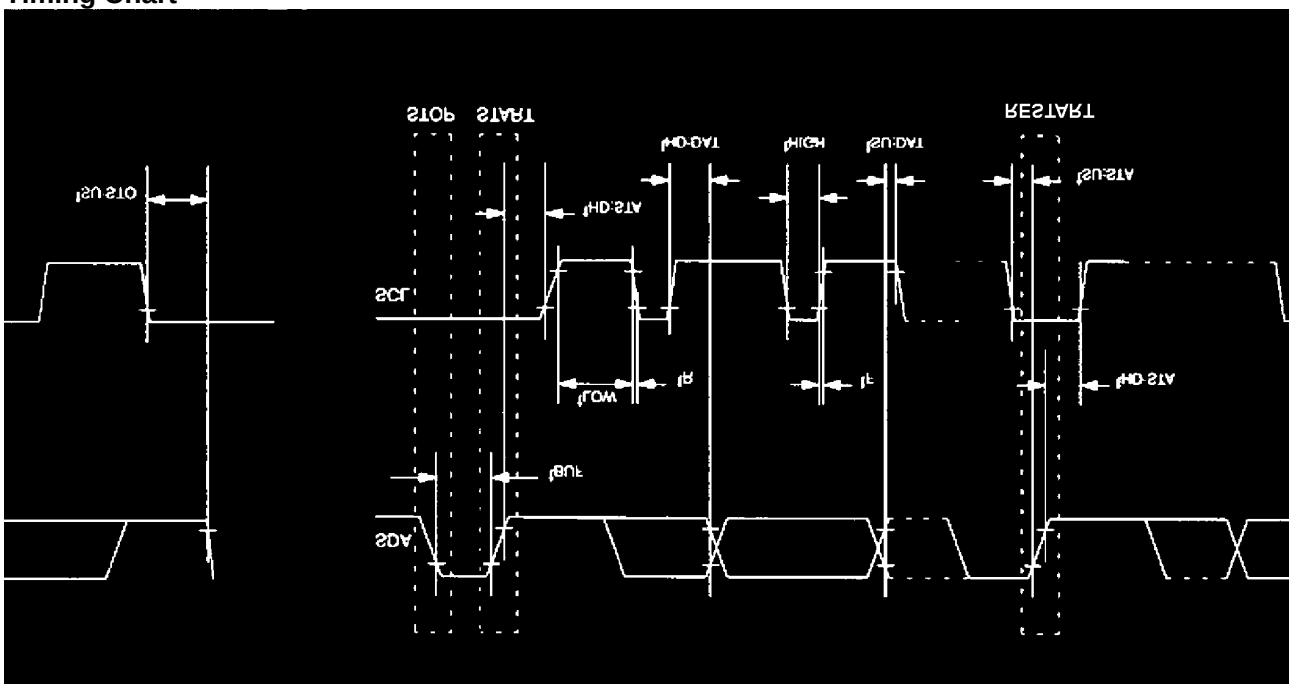
Parameter Description, Measurement Unit	Identification	Measurement Mode	Norm	
			min	max
Input leakage current, uA (SCL only)	I_{LI}	–	–	1
In / Out leakage current, uA (SDA and SQW/OUT)	I_{LO}	–	–	1
Low level output voltage, V	V_{OL} [1)]	V_{CC} = 4.5 V	–	0.4
Consumption current in the data transfer mode, µA	I_{CCA}	f_{SCL} = 100 kHz	–	1500
Consumption current in the static mode, µA	I_{CCS}	V_{CC} = 5 V and SDA, SCL = 5 V	–	200
Consumption current in the battery mode (SQW/OUT OFF., 32 kHz – ON), µA	I_{BAT1}	V_{CC} = 0 V, V_{BAT} = 3 V	–	0.5
Consumption current in the battery mode (SQW/OUT – ON, 32 kHz – ON), µA	I_{BAT2}	V_{CC} = 0 V, V_{BAT} = 3 V	–	0.8
Low level voltage is determined under the load current of 5 mA; V_{OL} = GND under the capacitance load				

Dynamic parameters of the microcircuit HT1307A (T_A = –40...+ 85°C, V_{CC} = 4.5 – 5.5

V) Parameter Description, Measurement Unit	Identification	Measurement Mode	Norm	
			Not less	Not more
Cycle frequency SCL, kHz	f_{SCL}	–	0	100
Time of the bus vacant status between the statuses of STOP and START, µsec	t_{BUF}	–	4.7	–
Hold time (repeated) of START status, µsec	$t_{HD:STA}$ 1)	–	4.0	–
Duration of the low status of the cycle pulse SCL, µsec	t_{LOW}	–	4.7	–
Duration of the cycle pulse high status SCL, µsec	t_{HIGH}	–	4.0	–
Pre-set time for the repeated status START, µsec	$t_{SU:STA}$	–	4.7	–
Data hold time, µsec	$t_{HD:DAT}$ 2)	–	0	–
Data pre-set time, nsec	$t_{SU:DAT}$	–	250	–
Rise time of signals SDA and SCL, nsec	t_R	–	–	1000
Drop time of signals SDA and SCL, nsec	t_F	–	–	300
Pre-set time for the status STOP, µsec	$t_{SU:STO}$	–	4.7	–
TotaL capacitance load per each bus line, pF	C_B	–	–	400
IN / OUT capacitance, pF	$C_{I/O}$	–	10	10
Load capacitance of the quartz resonator, pF	C_{LX}	–	12.5	12.5

After this time interval the first time cycle signal is formed;
Device should internally ensure the hold time, at least, 300 nsec for the signal SDA (relative to V_{IHMIN} of signal SCL) in order to overlap the indeterminancy area of the fall signal of SCL.
maximum value $t_{HD:DAT}$ should be definite in that case, if the device does not increase duration of the low status (t_{LOW}) of signal SCL.

Timing Chart



HT1307A Functioning

HT1307A operates as the driven device on the serial bus. For access to it it is required to set the status START and to send after the register address the device identification code. It is possible to address the next register consequently, until the status STOP is set. When V_{CC} drops below 1.25 x V_{BAT}, the access in progress to the device is ceased and the address counter is reset. At this time the device does not recognize the input data, excluding the erroneous information writing. When V_{CC} drops below V_{BAT}, the device switches over to the battery mode, consuming low power. When switching on the power supply V_{CC} above V_{BAT} + 0.2 V, the device switches over from the battery power supply to V_{CC}; and recognizes the input data, when V_{CC} becomes above 1.25 x V_{BAT}

Addresses Chart of RTC and RAM

Addresses chart of the registers RTC and RAM is indicated in the Figure. Hour registers of the real time are positioned at the addresses 00h – 07h. RAM registers are positioned at the addresses of 08h – 3Fh. In the mode of the multi-byte access, when reaching by the pointer of the address 3Fh, the end of the RAM address space, there happe ith the address 00h, beginning of the hours area.

00H	SECONDS
	MINUTES
	HOURS
	DAY
	DATE
	MONTH
	YEAR
07H	CONTROL
08H 3FH	RAM 56 x 8

Hours and Calendar

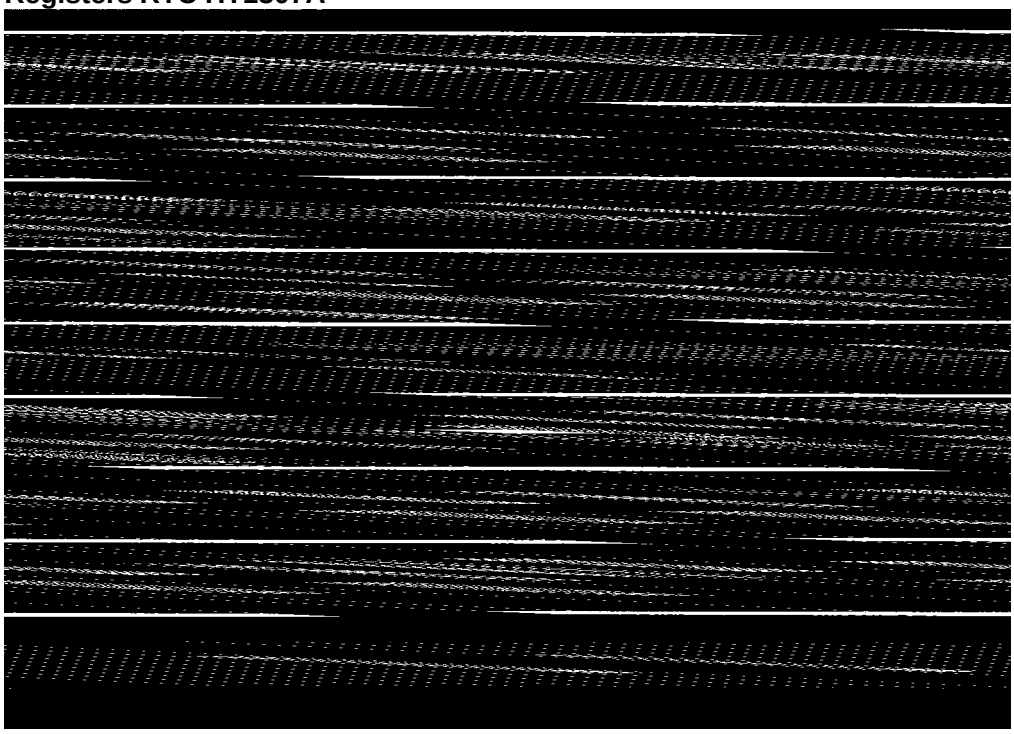
Information on the time and date is obtained by means of reading the appropriate register bytes. Hour registers of the real time are indicated in the Figure. Pre-setting and time and calendar initialization are performed by means of writing the appropriate bytes. Information, contained in the time and calendar registers, represents the binary-decimal code. Bit 7 of register 0 represents the hour stop bit (CH). When this bit is set to “1” , the generator is off.

When switching on the power supply, the initial status of all registers is not determined. It is necessary to enable the generator (bit CH = 0) when setting the initial configurations.

HT1307A operates in the 12-hour or in the 24-hour format. The bit 6 of the watch register determines the operational mode. 12-hour mode corresponds to the high level. In the 12-hour mode the bit 5 is the AM/PM bit. The high level corresponds to PM. In the 24-hour mode, the 5 is the second bit of tens of hours (20 -23 hours).

During application of the signal “START” to the two-wire bus there happens transfer of the real time to the auxiliary set of registers. The time data are read from these auxiliary registers, while the watch proceeds in operation. This eliminates the necessity of repeated reading in case of updating the basic registers in the access process.

Registers RTC HT1307A



Control Register

Control register is used for control of pin SQW/OUT.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (output control): This bit presets the output logic level of the pin SQW/OUT, when the output of the rectangular signal is locked.

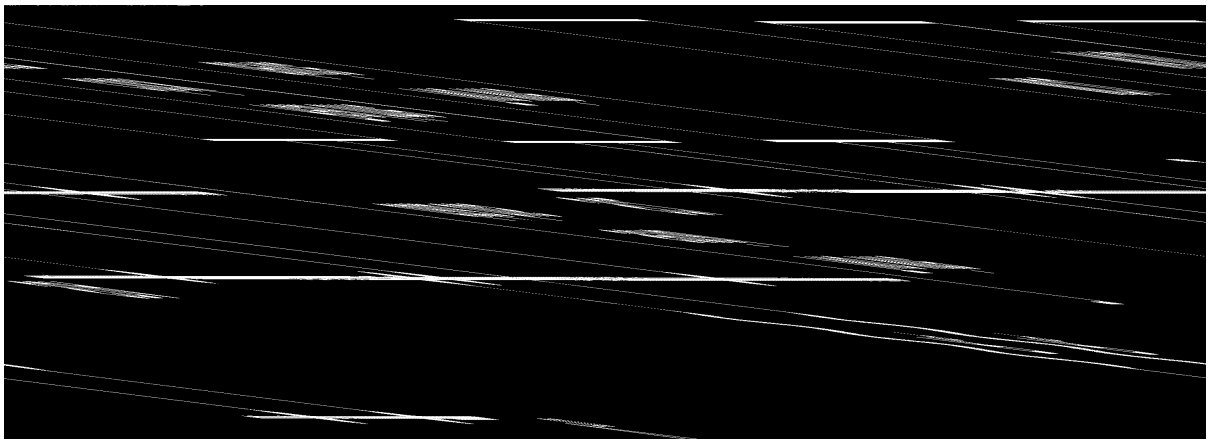
SQWE (rectangular signal enabling): This bit, pre-set to the logic “1”, activates the generator output. Frequency of the output rectangular signal is determined by the bits RS0 and RS1.

RS (frequency selection): These bits determine the frequency of the output rectangular signal, when the output of the rectangular signal is activated. The table indicates the frequencies, which can be selected by the bits RS.

RS1	RS0	Frequency SQW/OUT
0	0	1 Hz
0	1	4,096 kHz
1	0	8,192 kHz
1	1	32,768 кГц

Two-wire Serial Data Bus

HT1307A supports the bi-directional two-wire bus and the protocol of the data exchange. The bus can be controlled by the “master” device, which generates the cycle signal (SCL), controls access to the bus, generates the statuses START and STOP. Typical configuration of the bus with the two-wire protocol is indicated in Figure.



Data transfer can be initiated only when the bus is not occupied. In the process of the data transfer the data line should remain stable, while the line of the cycle signal is in the high status. Status alterations of the data line at that moment, when the cycle line is in the high status, will be regarded as the control signals.

In compliance with this the following conditions are determined:

Bus not occupied: both the data line and the cycle signal are in the HIGH status.

Data transfer start: Status alteration of the data line during transition from HIGH to LOW, while the cycle line is in the HIGH status, is determined as the status START.

Data transfer stop: Status alteration of the data line during transition from LOW to HIGH, while the cycle line is in the HIGH status, is determined as the status STOP.

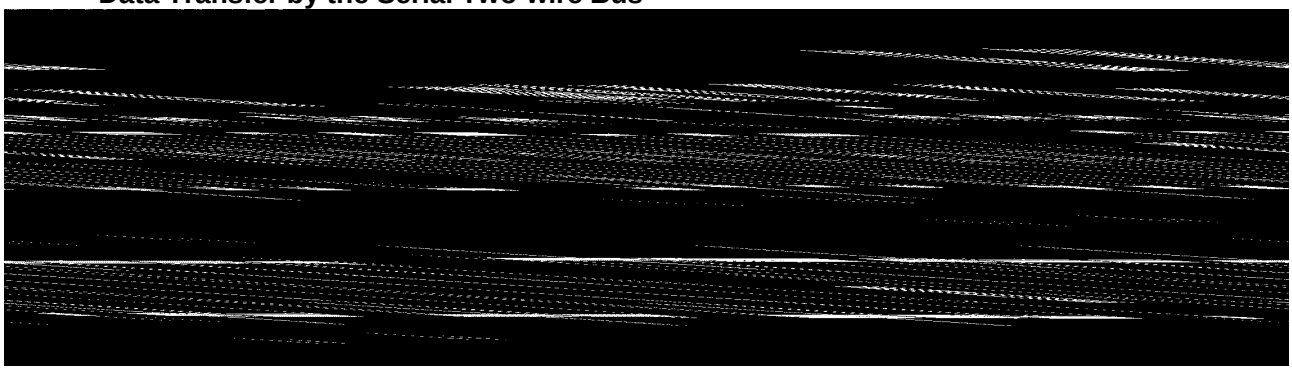
Valid data: Data line status complies with the valid data, when after the status START the data line is stable during the HIGH status of the cycle signal. Data on the line should be altered at the time of the LOW status of the cycle signal. One cycle pulse per one data bit.

Each data transfer starts at the beginning of the status START and ceases at the beginning of the status STOP. Number of the data bytes, transferred between the statuses START and STOP is not limited and is determined by the «master» device. Information is transferred byte by byte, and each receipt is confirmed by the ninth byte. HT1307A operates in the normal mode only (100 kHz).

Confirmation of receipt: Each receiving device, when it being addressed, has to generate the recept confirmation after receiving each byte. «Master» device should generate the cycle pulses, which are allocated in compliance with the confirmation bits.

If the receipt confirmation signal is in the high status, then on arrival of the confirmation cycle pulse, the device, confirming the receipt, should switch over the SDA line to the low status. Of course, there should be considered the pre-set time and the hold time. The «master» device should signalize on completion of the data transfer to the “slave” device, ceasing generation of the confirmation bit on receiving the receipt confirmation from the “slave” cycle pulse. In this case, the «slave one should switch over the data line to the low status, in order to enable the «master» one generate the condition of STOP.

Data Transfer by the Serial Two-wire Bus



Depending on the status of bit $R/\overline{W}$, there are possible two types of transfer:

1.**Data are transferred from the «master» transmitter to the «slave» receiver.** The first byte, transmitted by the «master» one, is the address for the «slave» one. Then follows a sequence of the data bytes. The «slave» one returns the receipt confirmation bytes after each received byte. Order of the data transfer: the first is the most senior digit (MSB).

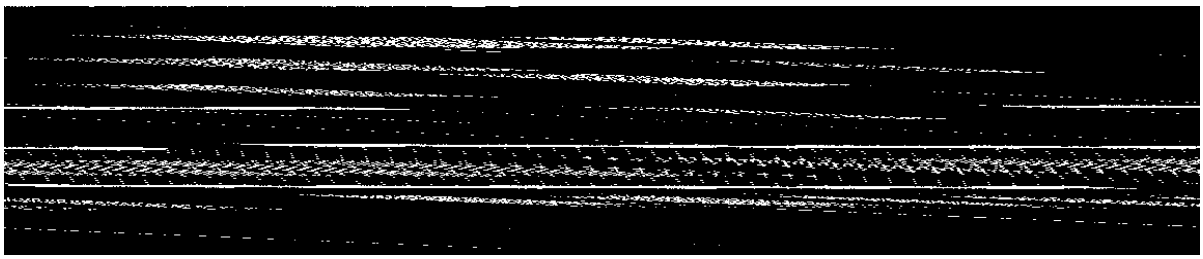
2. **The data are transferred from the «slave» transmitter to the «master» receiver.** The first byte (address of «slave») is applied to the «master». Then the «master» returns the confirmation bit. This follows after the transfer by the «slave» of the data sequence. The «master» returns the receipt confirmation bit after each received byte, with the exception of the last byte. After receipt of the last byte the receipt confirmation bit is not returned.

The «master» device generates all cycle pulses and the statuses START and STOP. Transfer is completed at emergence of the status STOP or the repeated emergence of the status START. As the repeated status START is the beginning of the next serial transfer, the bus is not vacated.The data transfer order: the first is the most senior digit (MSB).

HT1307A can operate in the two following modes:

1.**Mode of «slave» receiver (write mode of HT1307A):** Serial data and cycles are received via SDA and SCL appropriately. After transfer of each byte the confirmation bit is sent. The statuses START and STOP are recognized as the beginning and the end of the serial transfer. The address recognition is performed by means of the hardware after receipt of the “slave” address and the direction bit. The address byte isthe first byte, received after occurrence of the START status, generated by the “master”. The address byte contains the seven address bits of HT1307A, equal to 1101000, accompanied by the direction bit (R/W), which for write is equal to 0.After receipt and decoding of the address byte, DS1307 applies confirmation to the line SDA. After confirmation by HT1307A of the “slave” address and the write bit, the «master» sends the register address of HT1307A . Thus the register indicator will be preset in HT1307A. Then the «smart» shall start to send each data byte with the subsequent receipt confirmation of each byte. Upon completion of writing the “master” shall formulate the status STOP for termination of the data transfer.

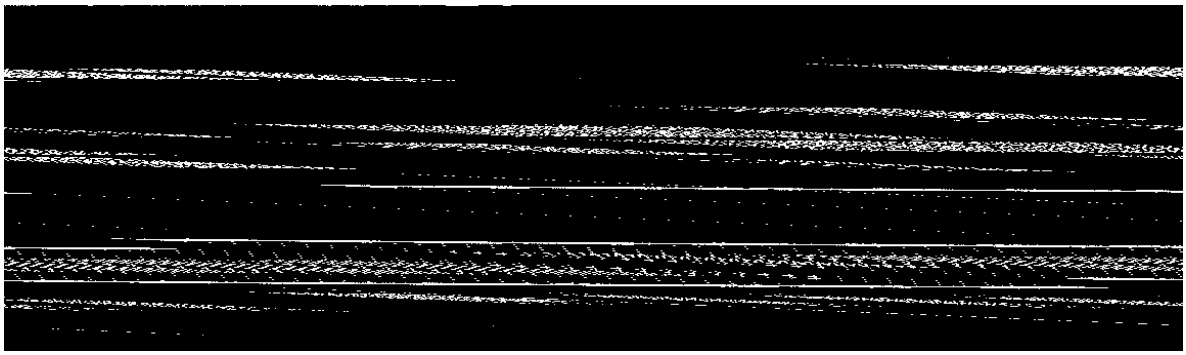
Data writing – mode of «slave» receiver



2. **Mode of «slave» receiver (write mode from HT1307A):** The first byte is received and processed as in the mode of the «slave» receiver. However, in this mode the direction bit will signify, that the transmission direction is changed. HT1307A sends the serial data by SDA, the cycle pulses - by SCL. statuses START and STOP are understood as the beginning and end of the consecutive transmission. The address byte is the first byte, received after occurrence of the status START,

generated by the «master». The address byte contains the seven bits of the address DS1307, equal to 1101000, accompanied by the direction bit ($R/\overline{W}$), which is equal to 1 for reading. After receipt and decoding of the address byte HT1307A receives confirmation from the line SDA. Then HT1307A starts to send the data from the address, which is indicated by the register indicator. If the register indicator is not written prior to initialization of the read mode, then the first read address is the last address , retained in the register indicator. HT1307A should send the bit of «non-confirmation», in order to complete the reading.

Data reading – mode of «slave» transmitter



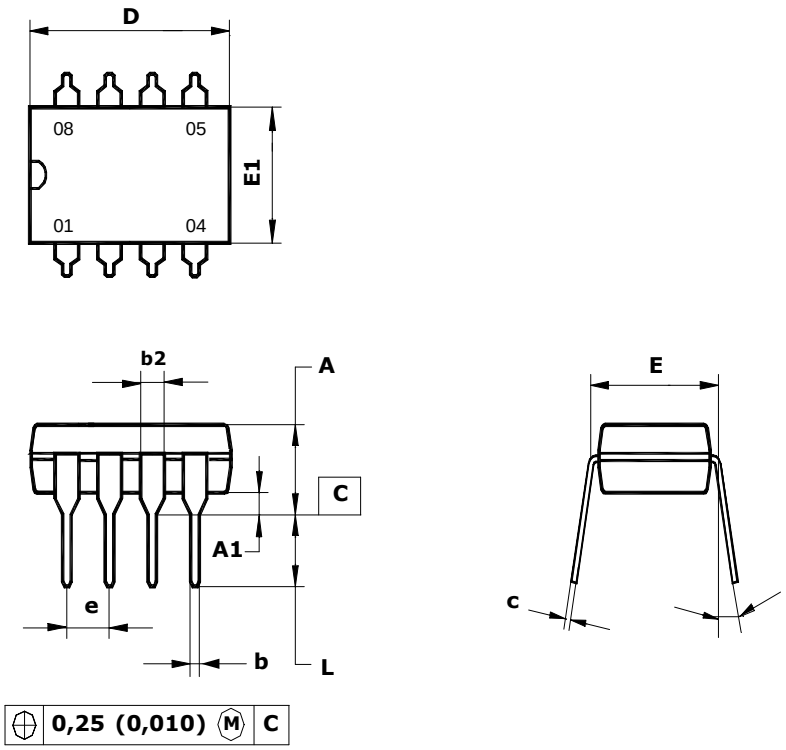
Designation of Pins HT1307A

Number of	Package Pin Identification	Type	Pin Designation
1	X1	In	Pin for connection of the quartz resonator
2	X2	In	Pin for connection of the quartz resonator
3	VBAT	In	Pin for battery
4	GND	In	Ground pin
5	SDA	Bi	Input / output of serial data
6	SCL	In	Input of the consecutive cycle signal
7	SQW/OUT	Out	Output of rectangular signal
8	VCC	In	Power supply pin

Package Overall Dimensions

PLASTIC DIP

(MS-001BA)



Note - Dimensions D, E1 do not include the fin value, which should not exceed 0.25 (0.010) per one side.

	D	E1	A	b	b2	e	α	L	E	c	A1
Millimeters											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
Inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—