16-bit Serial-In/Parallel-Out Constant-Current LED Driver

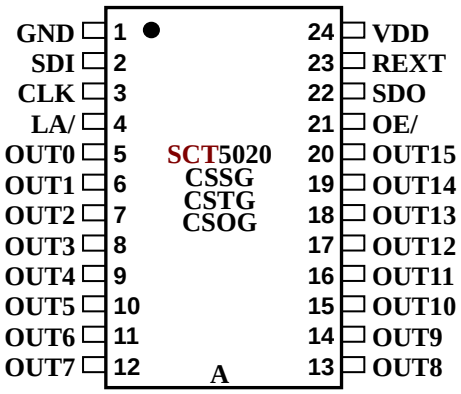
Product Description

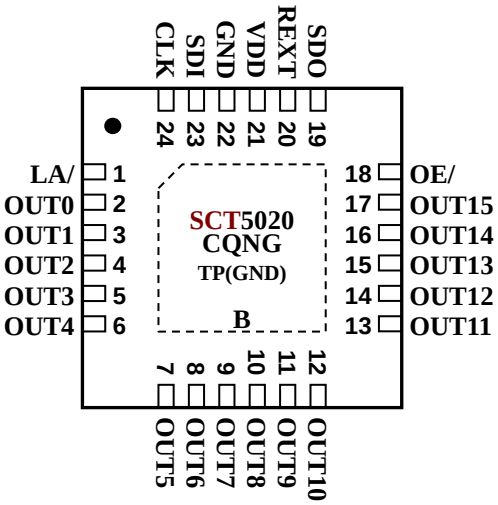
The SCT5020 serial-interfaced LED driver sinks 16 LED clusters with constant current to keep the uniform intensity of LED displays. In applications, an external resistor is used to set the full-scale constant output current from 5mA up to 45mA. The SCT5020 guarantees each output can endure maximum 17V DC voltage stress. The built-in shift registers and data latches making the SCT5020 effective solution in driving LED display. The output enable function gates all 16 outputs on and off, and is fast enough to be used as PWM input for LED intensity control. Since the serial data input rate can be reached up to 25MHz, the SCT5020 will satisfy system which needs high volume data transmission to control the LED display. Furthermore, the SCT5020 provides excellent temperature regulation thus it can be applied to varied of operating temperature.

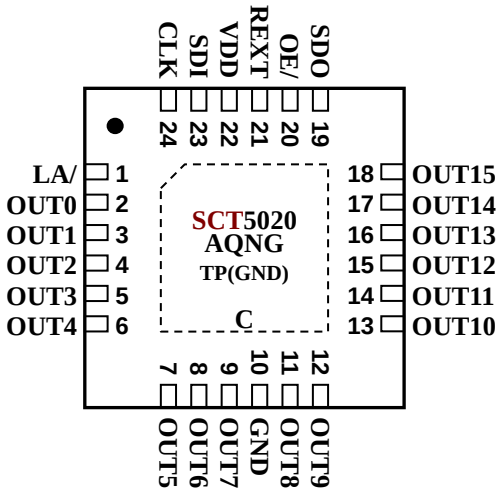
Features

- Finest grayscale response with 40ns PWM pulse width
- 16 robust constant current sinker with LED power-supply voltage up to 17V
- Constant output current : 5 – 30/45mA@3.3/5V
- Wide power supply voltages: 3.3V to 5V
- Excellent regulation to load, supply voltage and temperature
  Load regulation: ±0.1%/V
  Line regulation: ±0.5%/V
- High current matching accuracy: ±1% between outputs, ±2% between ICs
- Dropout voltage 0.5V@20mA, V_{DD}=5V
- CMOS Schmitt trigger inputs with clock rate up to 25MHz @ cascade connection
- The constant current value of 16 outputs is set by a single external resistor
- Built-in power on reset(POR) circuit forces all the outputs off while power on
- Package: SSOP24, SSOP24-1, SOP24 and TQFN24
- Applications: LED Displays, Variable Message Signs, Illumination, LED Traffic Signs

Pin Configurations



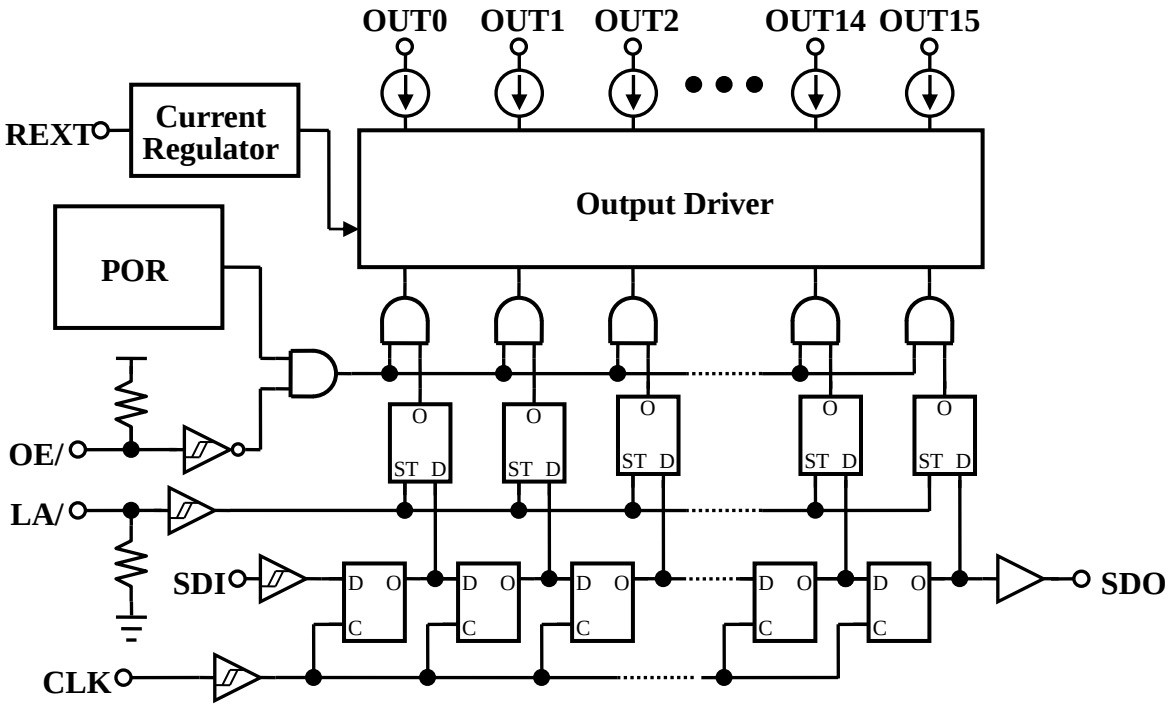




Terminal Description

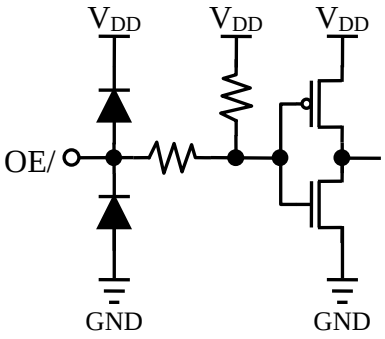
Pin Name	Pin No.			I/O	Function
	A	B	C		
GND	1	22 (TP)	10 (TP)	-	Ground terminal(thermal pad included)
SDI	2	23	23	I	Serial input of data shift register.
CLK	3	24	24	I	Clock input of shift register, data is sampled at the rising edge of CLK.
LA/	4	1	1	I	Input terminal of data strobe. Data is latched when LA/ is low. And data on shift register goes through when LA/ is high.
OUT[0:15]	5-20	2-17	2-9 11-18	O	Open-drain, constant-current outputs.
OE/	21	18	20	I	Output enable signal. Output is enabled when OE/ is forced to low.
SDO	22	19	19	O	Output terminal of serial-data output to the SDI of next SCT5020.
REXT	23	20	21	I/O	Used to connect an external resistor for setting up all output current
VDD	24	21	22	-	Supply voltage terminal

Block Diagram

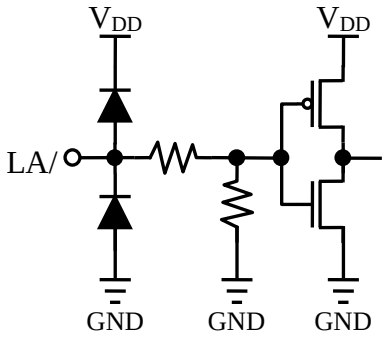


SCT5020

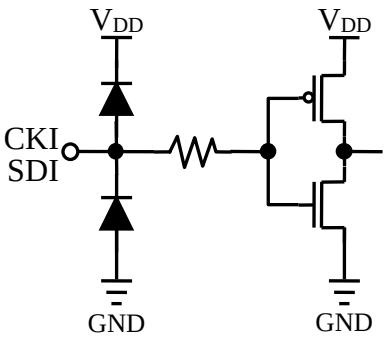
Equivalent Circuits of Inputs (1)



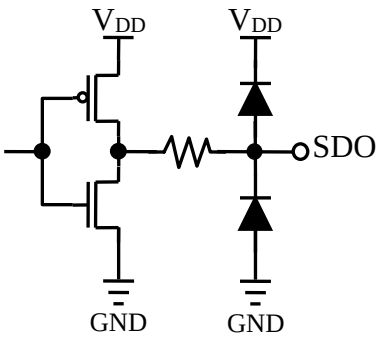
Equivalent Circuits of Inputs (2)



Equivalent Circuits of Inputs (3)



Equivalent Circuits of Output



Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT5020CSSG	SCT5020CSSG	Green SSOP24	2500
SCT5020CSTG	SCT5020CSTG	Green SSOP24-1	2000
SCT5020CSOG	SCT5020CSOG	Green SOP24	1000
SCT5020CQNG	5020CQNG	Green TQFN24	3000
SCT5020AQNG	5020AQNG	Green TQFN24	3000

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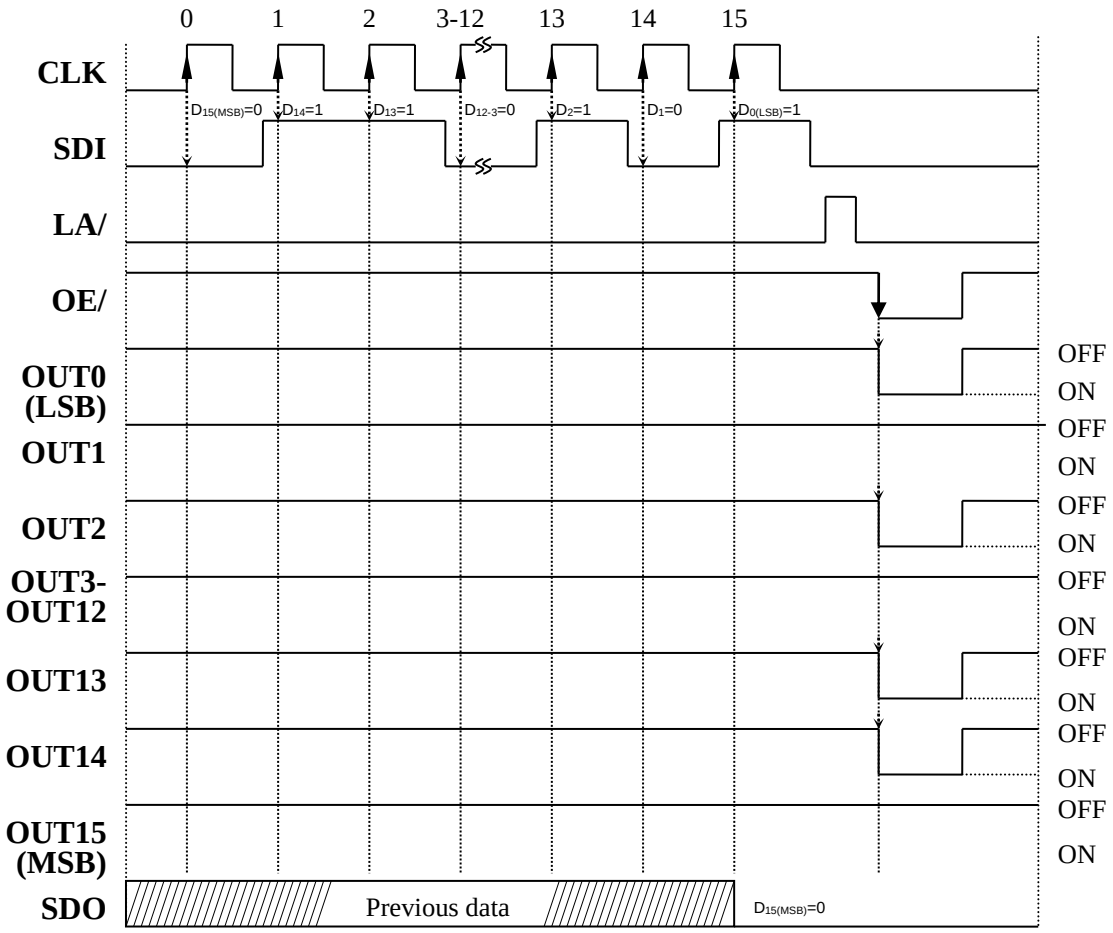
Truth Table

CLK	LA/	OE/	SDI	OUT0 ~ OUT15	SDO
↑	H	L	D_n	D_n D_{n-1} ---- D_{n-14} D_{n-15}	D_{n-15}
↑	L	L	D_{n+1}	No change	D_{n-14}
↑	H	L	D_{n+2}	D_{n+2} D_{n+1} ---- D_{n-12} D_{n-13}	D_{n-13}
↓	X	L	D_{n+3}	D_{n+2} D_{n+1} ---- D_{n-12} D_{n-13}	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Timing Diagram



Maximum Ratings (T_A = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{DD}	7.0	V
Input voltage		V_{IN}	-0.2 to V_{DD}+0.2	V
Output current		I_{OUT}	60	mA/Channel
Output voltage	SDO	V_{OUT}	-0.2 to V_{DD}+0.2	V
	OUT0~OUT15		-0.2 to 17	V
Total GND terminals current		I_{GND}	960	mA
Power dissipation	SOP24	P_D	1.92	W
	SSOP24		1.42	
	SSOP24-1.0		1.74	
	TQFN24		2.08	
Thermal resistance	SOP24	$R_{TH(j-a)}$	65	°C /W
	SSOP24		88	
	SSOP24-1.0		72	
	TQFN24		60	
Operating junction temperature		$T_{J(max)}$	150	°C
Operating temperature		T_{OPR}	-40 to +85	°C
Storage temperature		T_{STG}	-55 to +150	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_A= -40 to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3	-	5.5	V
Output voltage	V_{OUT}	Output OFF	-	-	17	V
		Output ON	-	1[1]	4[2]	V
Output current	I_{OUT}	V_{DD}=3.3/5V	5	-	30/45	mA
Input voltage	V_{IH}	Input signals	0.7V_{DD}	-	V_{DD}	V
	V_{IL}	Input signals	0	-	0.3V_{DD}	V
OE/ pulse width	$t_{W(OE)}$	V_{DD}=3.3V/5V	180	-	-	ns

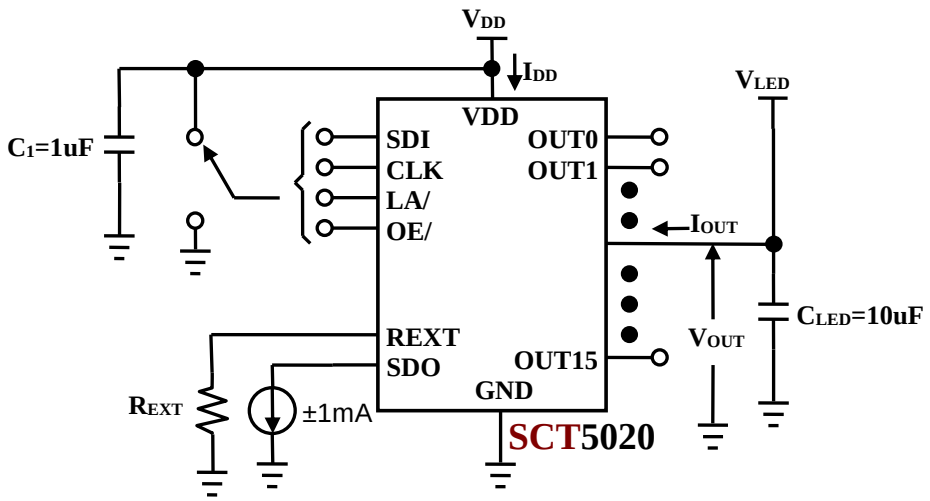
1. The output current keep constant in range of 5-45mA if V_{OUT}=1V.
   However, user can minimize V_{OUT} to reduce power dissipation according to used current, e.g., set V_{OUT} to 0.6V if I_{OUT}=20mA.
2. The maximum Vout is package thermal limited, user should keep Vout under maximum power dissipation.

Electrical Characteristics (V_{DD}=3.3/5V, T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage		V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
		V_{IL}	-	0	-	0.3V_{DD}	V
SDO output voltage		V_{OH}	V_{DD}=3.3/5V, I_{OH}= -1mA	V_{DD}-0.4	-	-	V
		V_{OL}	V_{DD}=3.3/5V, I_{OL}=+1mA	-	-	0.4	V
Output leakage current		I_{OL}	V_{OUT}=17V	-	-	0.5	uA
Output current		I_{OUT}	V_{OUT}=1V, R_{EXT}=900Ω	-	20.5	-	mA
Current bit skew[1]		dI_{OUT1}	V_{OUT}=1V, R_{EXT}=900Ω	-	±1	±2	%
Chip skew[2]		dI_{OUT2}	V_{OUT}=1V, R_{EXT}=900Ω	-	±2	±3	%
Line regulation[3] I_{OUT} vs. V_{DD}		%/dV_{DD}	3V<V_{DD}<5.5V, V_{OUT}>1V, R_{EXT}=900Ω	-	±0.5	±1	%/V
Load regulation[4] I_{OUT} vs. V_{OUT}		%/dV_{OUT}	1V<V_{OUT}<4V, I_{OUT}=20.5mA, R_{EXT}=900Ω	-	±0.1	±0.5	%/V
Pull-up resistor		R_{UP}	OE/	-	400	-	KΩ
Pull-down resistor		R_{DOWN}	LA/	-	400	-	KΩ
Supply current	OFF	$I_{DD(OFF)1}$	V_{DD}=3.3/5V, R_{EXT}=Open, OUT[0:15]=OFF(to VCC)	-	3	4	mA
	OFF	$I_{DD(OFF)2}$	V_{DD}=3.3/5V, R_{EXT}=900Ω, OUT[0:15]=OFF(to VCC)	-	5	7	mA
	ON	$I_{DD(ON)}$	V_{DD}=3.3/5V, R_{EXT}=900 Ω, OUT[0:15]=ON	-	8	10	mA

1. Bit skew=(I_{OUT}-I_{AVG}) / I_{AVG}, where I_{AVG}=($I_{OUT(max)}$+ $I_{OUT(min)}$)/2
2. Chip skew=(I_{AVG}-I_{CEN}) / I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.
3. Line regulation=[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)] / {[I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2} / (5.5V-3V)*100(%/V)
4. Load regulation=[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)] / {[I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2} / (4V-1V)*100(%/V)

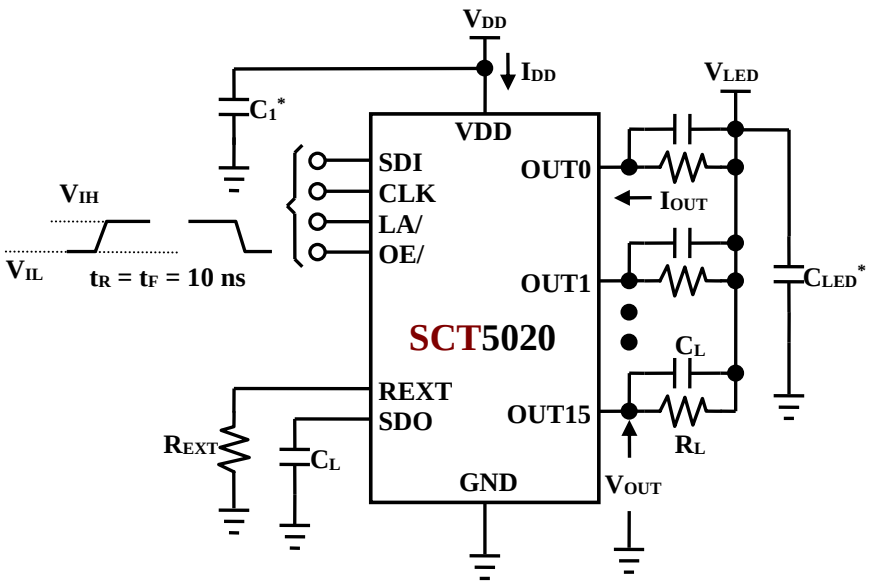
Test Circuit for Electrical Characteristics



Switching Characteristics (T_A=25°C unless otherwise noted)

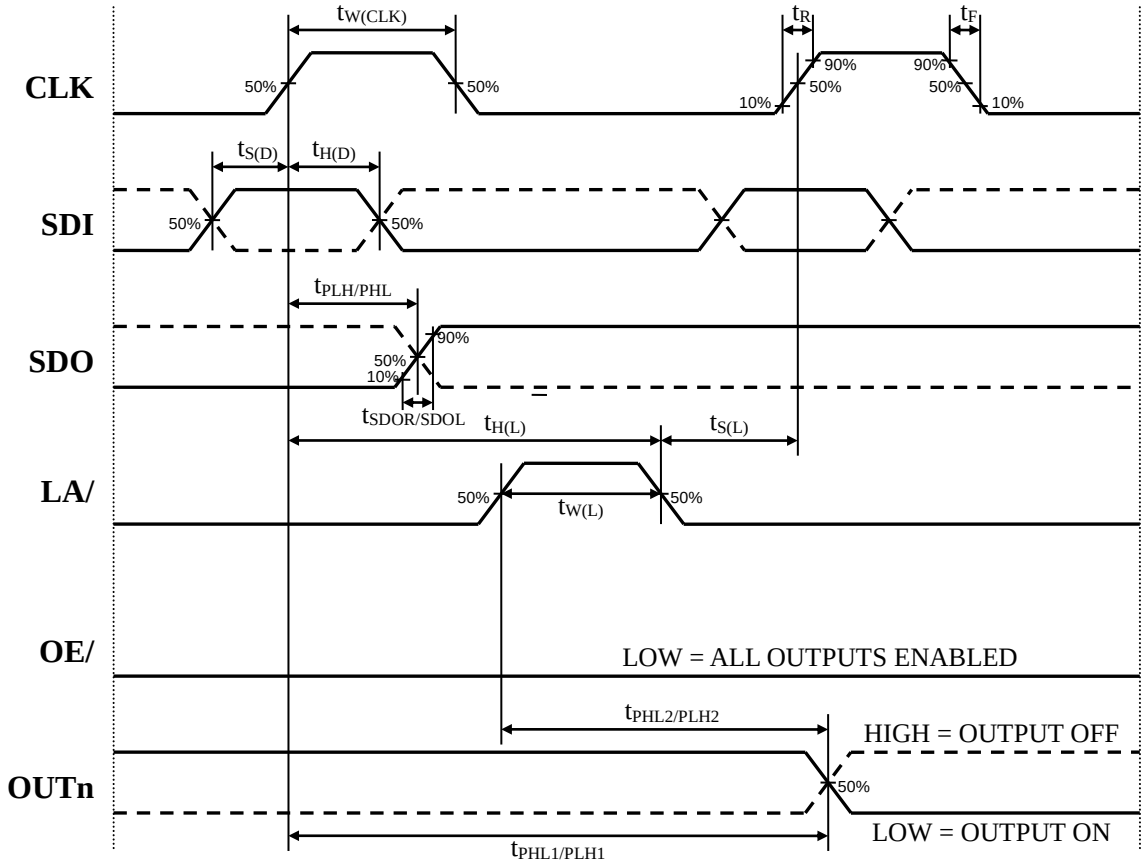
Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time (“L” to “H”)	CLK - OUTn	t_{PLH1}	V_{DD} = 3.3/5V V_{LED} = 5V V_{IH} = V_{DD} V_{IL}= GND R_{EXT} = 900Ω R_L = 180Ω C_L = 10pF C_1 = 1uF C_{LED} = 10uF	-	80	150	ns
	LA/ - OUTn	t_{PLH2}		-	80	150	ns
	OE/ - OUT0	t_{PLH3}		-	80	150	ns
	CLK - SDO	t_{PLH}		-	20	40	ns
Propagation delay time (“H” to “L”)	CLK - OUTn	t_{PHL1}		-	80	150	ns
	LA/ - OUTn	t_{PHL2}		-	80	150	ns
	OE/ - OUT0	t_{PHL3}		-	80	150	ns
	CLK - SDO	t_{PHL}		-	20	40	ns
Pulse width	CLK	$t_{W(CLK)}$		20	-	-	ns
	LA/	$t_{W(L)}$		20	-	-	ns
	OE/	$t_{W(OE)}$		50	-	-	ns
Setup time for SDI		$t_{S(D)}$		5	-	-	ns
Hold time for SDI		$t_{HD)}$		15			ns
Setup time for LA/		$t_{S(L)}$		5	-	-	ns
Hold time for LA/		$t_{H(L)}$		5	-	-	ns
SDO rise time		t_{SDOR}		-	10	-	ns
SDO fall time		t_{SDOF}		-	10	-	ns
Output rise time of I_{OUT}		t_{OR}		-	40	60	ns
Output fall time of I_{OUT}		t_{OF}		-	40	60	ns
Slow CLK rise time[1]		t_R	Cascade	-	-	500	ns
Slow CLK fall time		t_F		-	-	500	ns

Test Circuit for Switching Characteristics

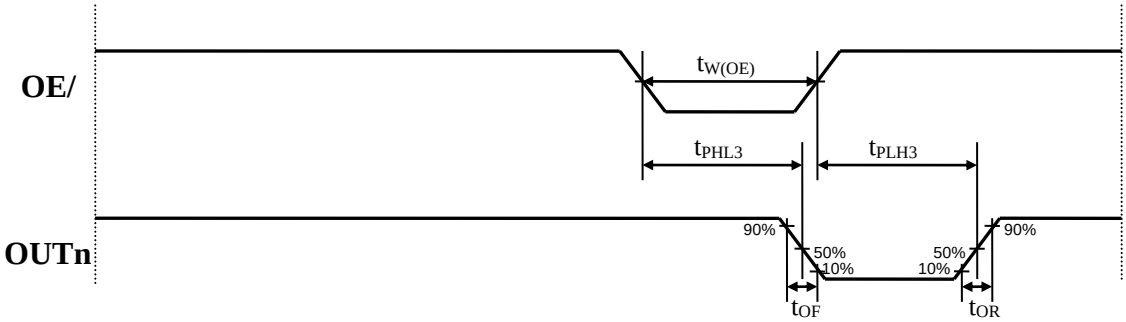


Timing Waveform

LA/ Control Output

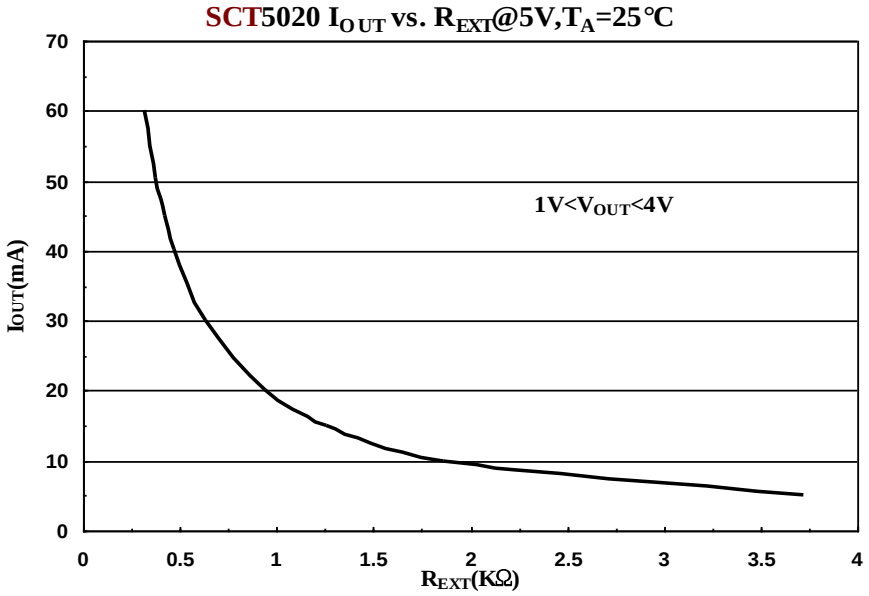


OE/ Control Output



Adjusting Output Current

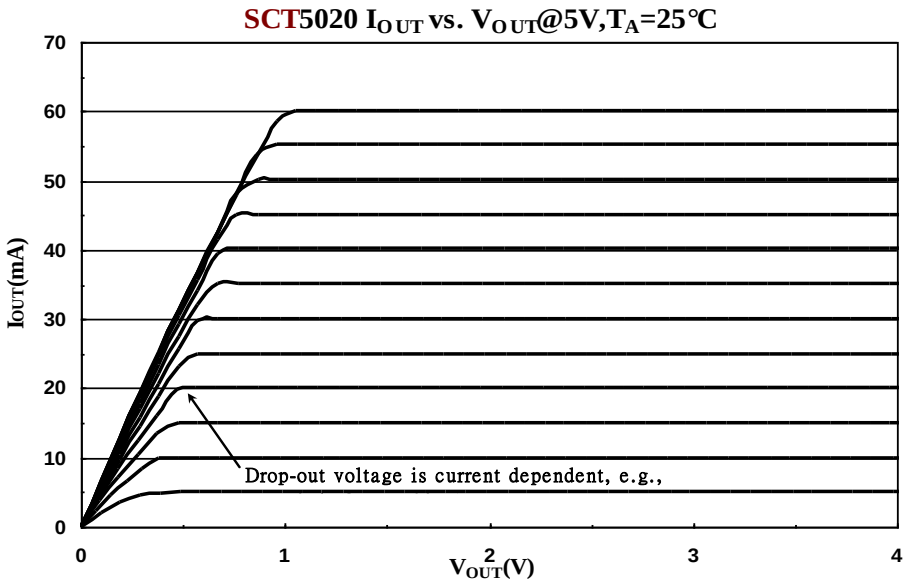
The SCT5020's output current (I_{OUT}) are set by one external resistor at pin REXT. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

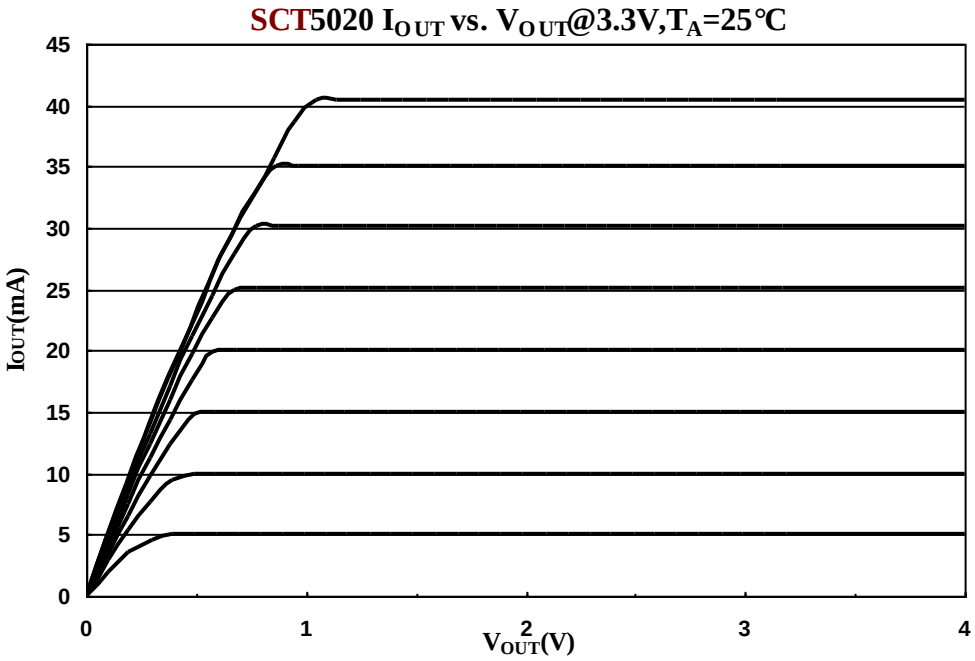


According to I-V curve of the output of SCT5020, the output voltage should be larger than 1V to get 45 mA constant current. By applying proper output voltage, the output current set by an external resistor is approximate to: I_{OUT} = 30(615 / REXT) (mA) (chip skew < ±3%). Thus the output current is set to be about 20.5mA at REXT = 900Ω.

Output Characteristics

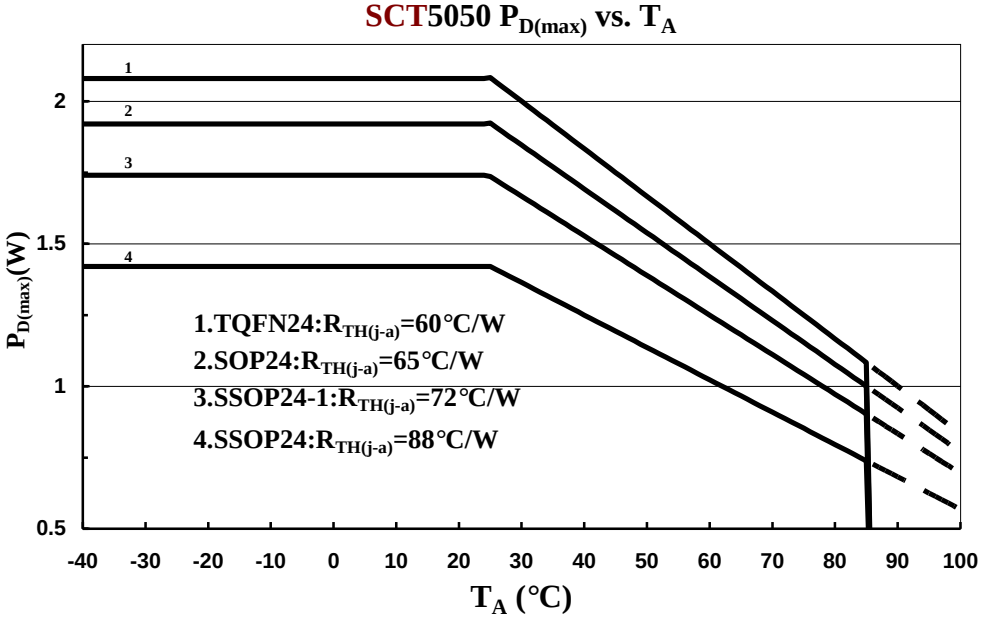
The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when $V_{OUT} > V_{DO}$ (Drop-Out voltage). The relationship between I_{OUT} and V_{OUT} is shown below. The output voltage should be kept as low as possible to prevent the SCT5020 from being overheated.





Power Dissipation

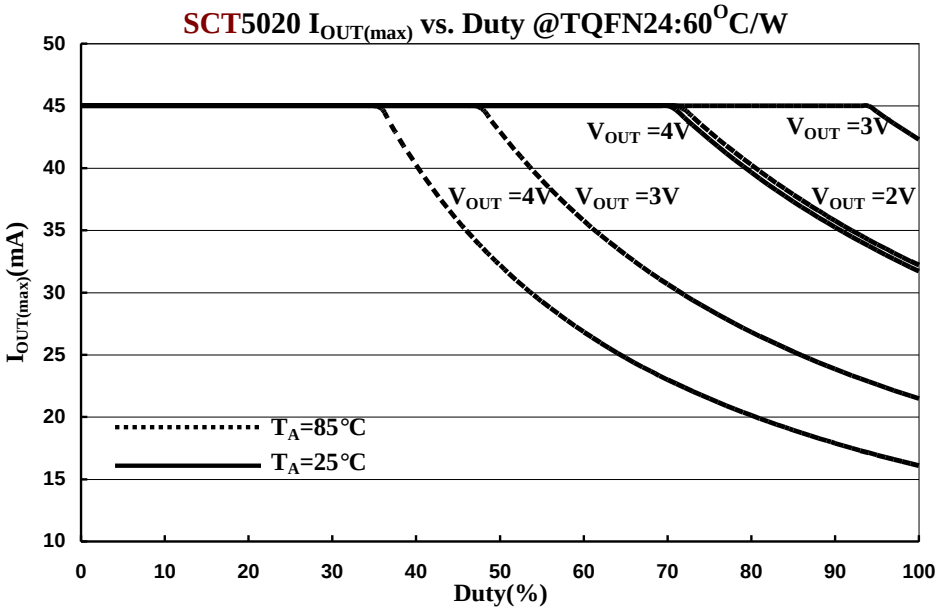
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)} - T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A: ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sinking larger I_{OUT}, users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT5020.

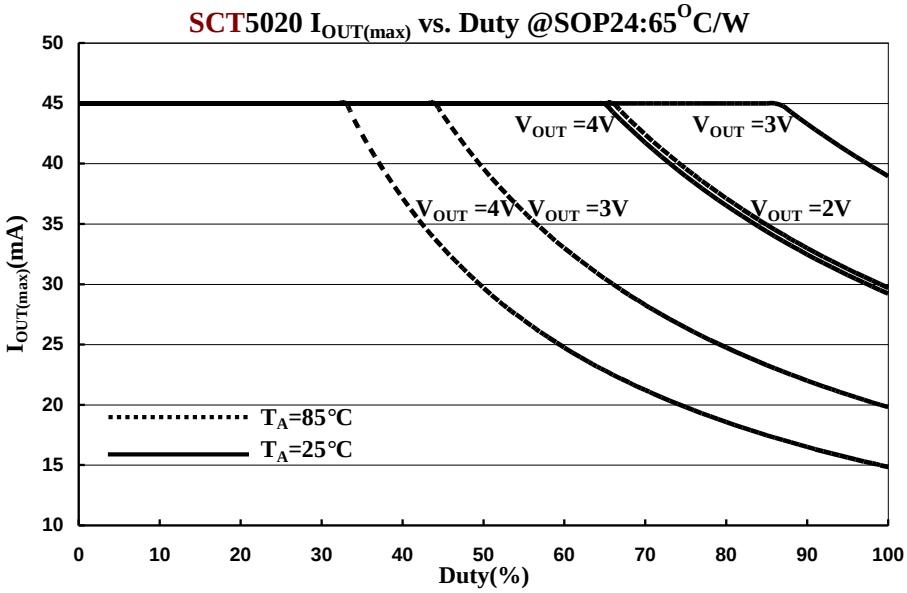


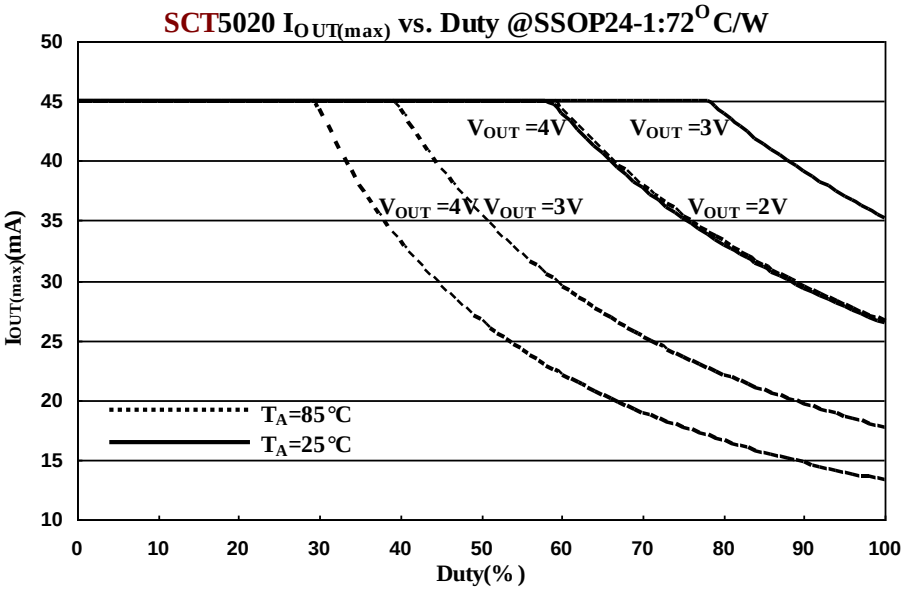
Limitation on Maximum Output Current

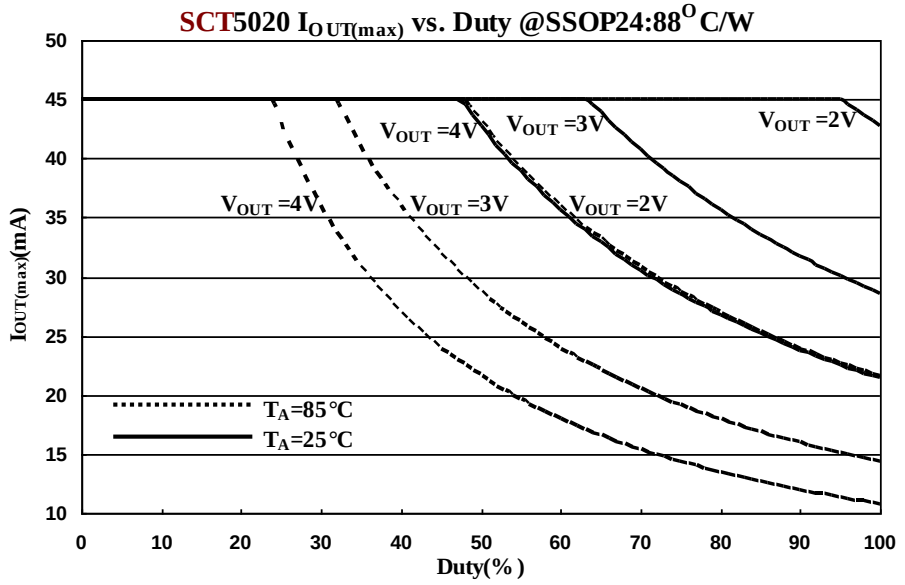
The maximum output current vs. duty cycle is estimated by:

$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(V_{DD}*I_{DD}))/V_{OUT}/Duty/N$ where $T_{J(max)}=150°C$, N=16(all ON)



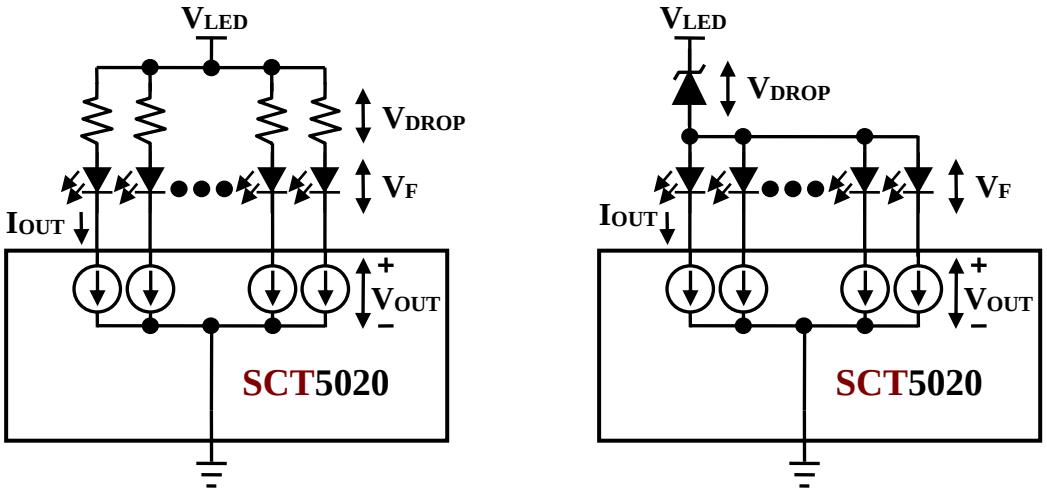




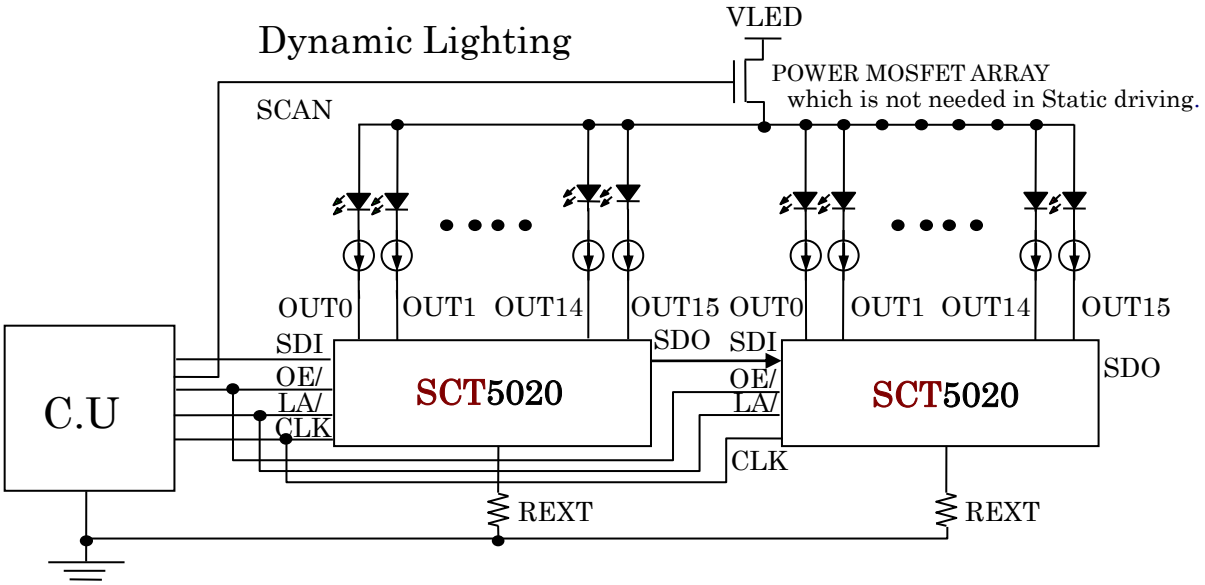


Load Supply Voltage (V_{LED})

The SCT5020 can be operated very well when V_{OUT} ranges from 1V to 4V. However, it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT5020. Suggested V_{OUT} is to be set greater than V_{DO} and less than 1V. The V_{DO} is dependent on the I_{OUT} current as indicated in section “Output Characteristics”. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.



Typical Application Circuits

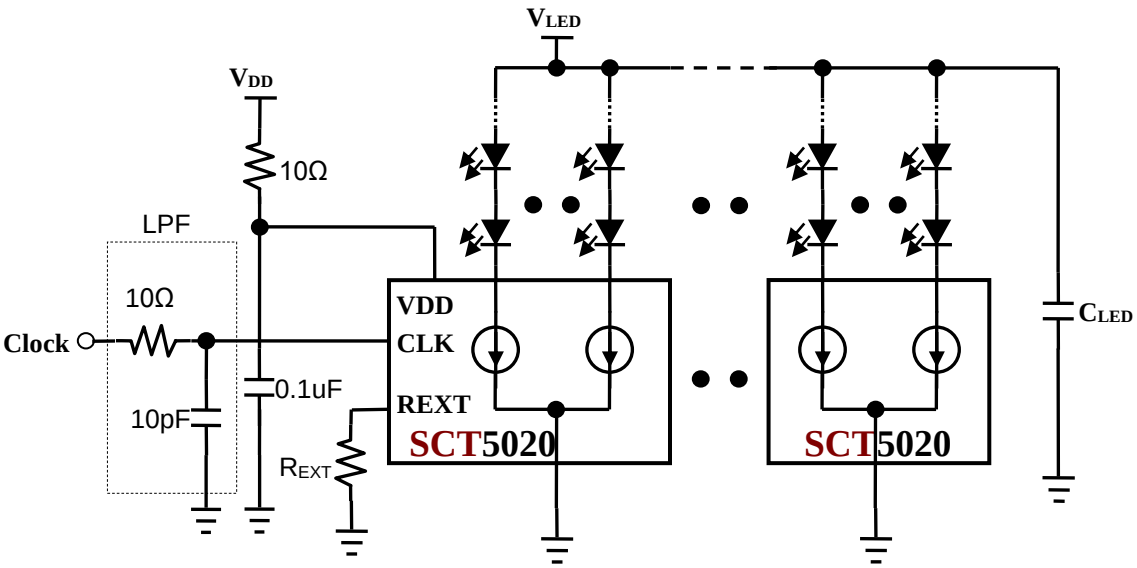


PCB Design Considerations

Use the following general guide-line when designing printed circuit boards **(**PCB**):**

Decoupling Capacitor

Place a decoupling capacitor e.g. 1uF between VDD and GND pins of SCT5020. Locate the capacitor as close to the SCT5020 as possible. This is normally adequate for static LED driving. For dynamic scan or PWM applications, it is suggested to add an additional capacitor of 4.7uF or more to each supply for every SCT5020. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



External Resistor (R_{EXT})

Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

Power and Ground

Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if I_{OUT} is larger) series in power input of the SCT5020 in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V_{LED}, furthermore adding a capacitor C_{LED} greater than 10uF beside the LED are recommended. Please adapt C_{LED} according to total system current consumption.

EMI Reduction

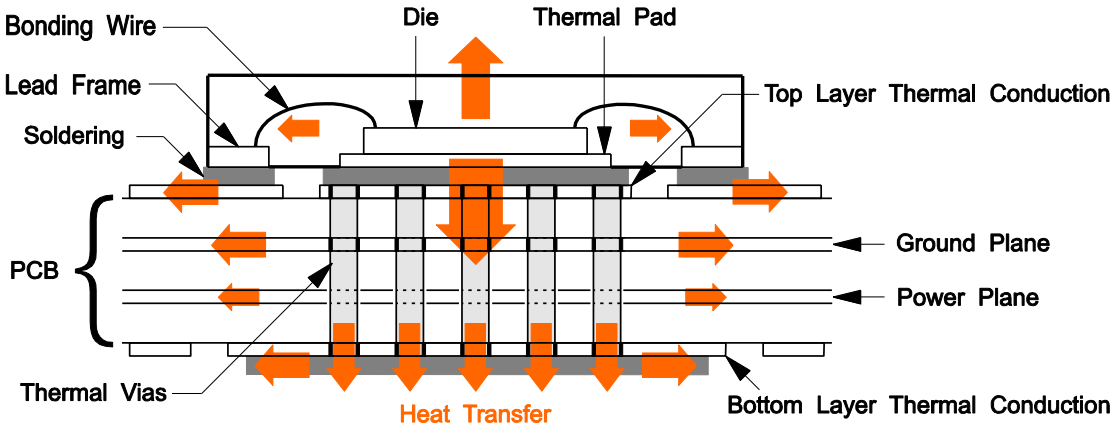
To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

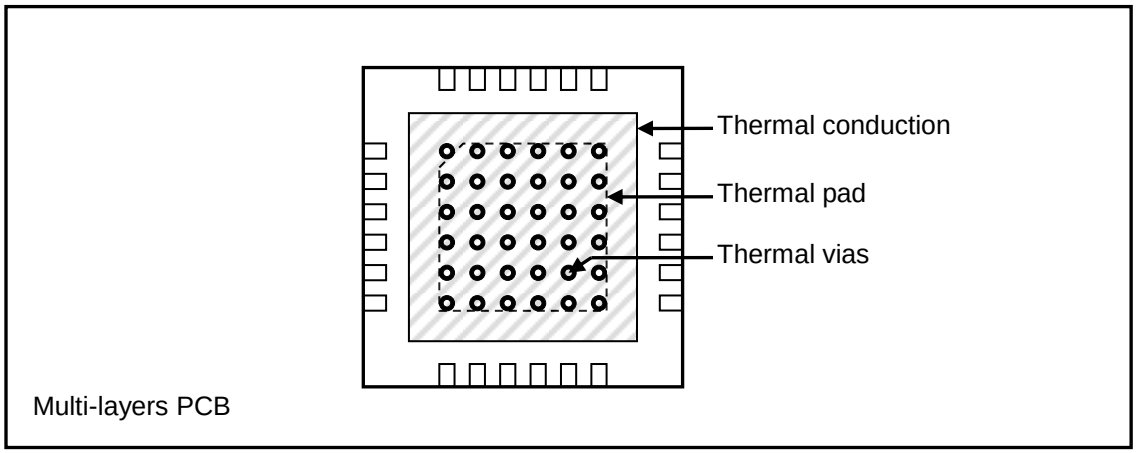
Thermal Pad Consideration

The “thermal pad” (also named as “exposed pad”) TQFN package beneath used to increase the heat dissipation capability is grounded. User should be aware of this electrical connection when designing the PCB board, and make provisions for its use. In most of application, the thermal pad is electrically connected to ground plane or conduction. This makes the IC operated with more stable condition.

In general, the heat generated from an IC is conducted to the PCB then radiates to the ambient. Thermal pad specifically increases the maximum power dissipation capability of the IC packages. To provide lower thermal resistance from the IC to the ambient air, PCB designers should layout larger thermal conduction areas on top layer (component side) and bottom layer (solder side) as well as thermal vias, the more the better. In addition, connecting thermal via to the ground plane also increases thermal conduction areas, this improves the heat transfer efficiency at the same time greatly dissipates heat generated from the package. Furthermore, coating solder on bottom layer and selecting, e.g., 2 oz. copper which will increase the total thickness of thermal conduction is an alternative.

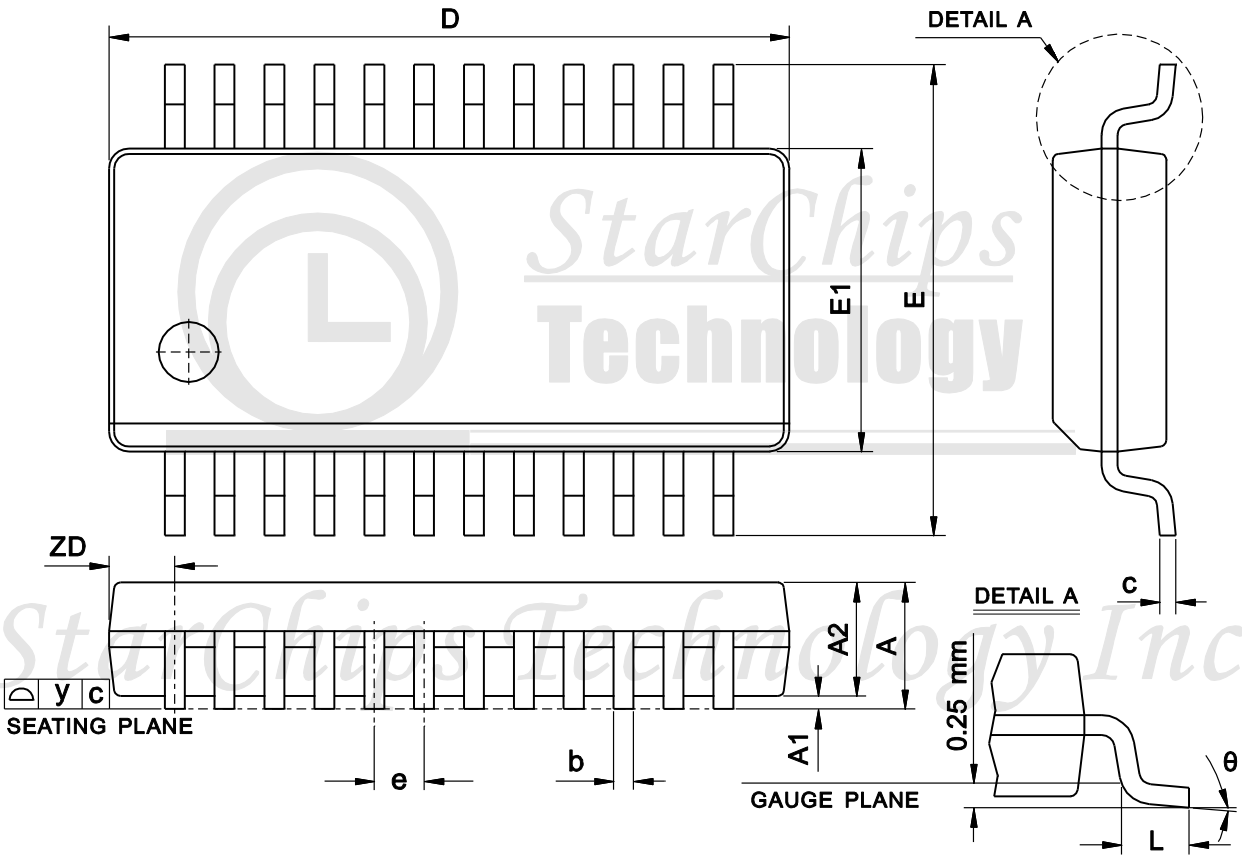
When making the solder paste screen, an opening should be created for the thermal pad. This way the thermal pad can be electrically and thermally connected to the PCB. As the thermal pad is soldered on copper polygon, the chance of inadvertently shorting the thermal pad to traces routed underneath it could be eliminated.





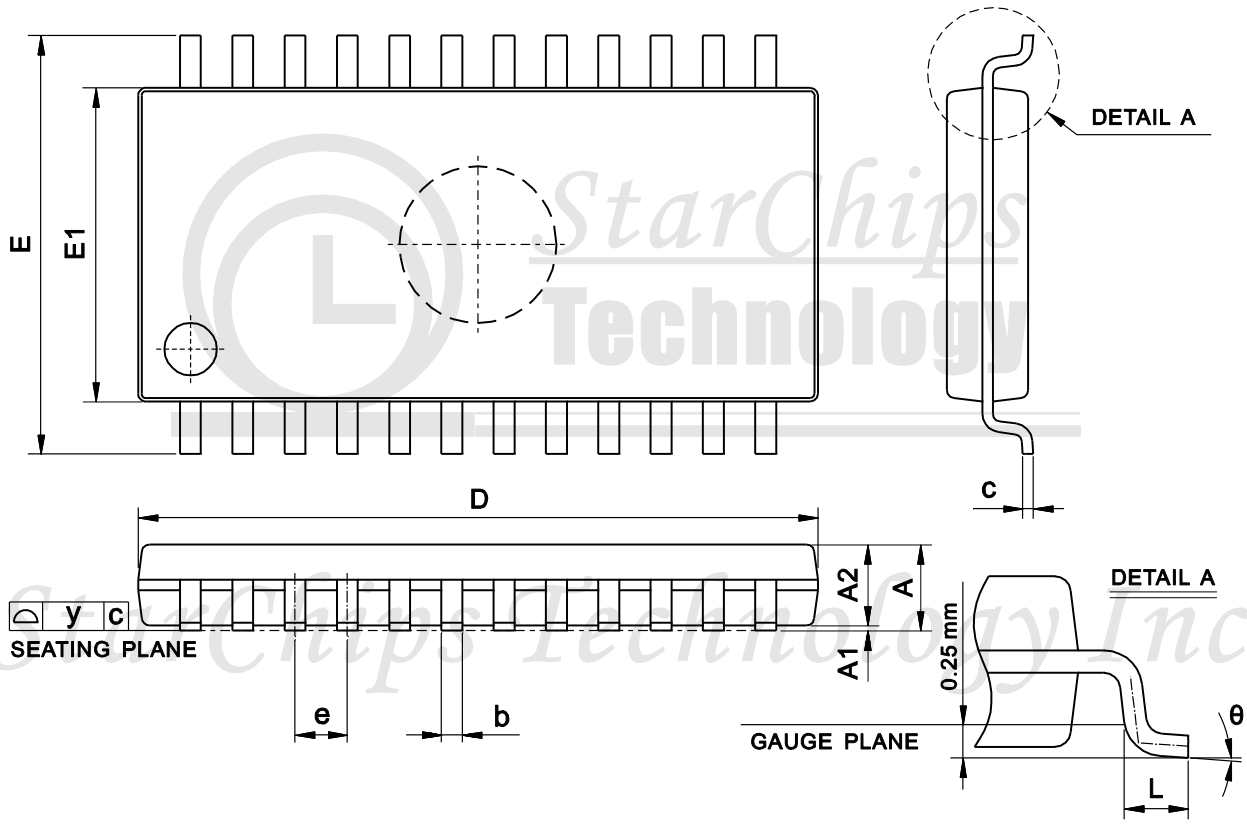
Package Dimension

SSOP24(check up-to-date version)



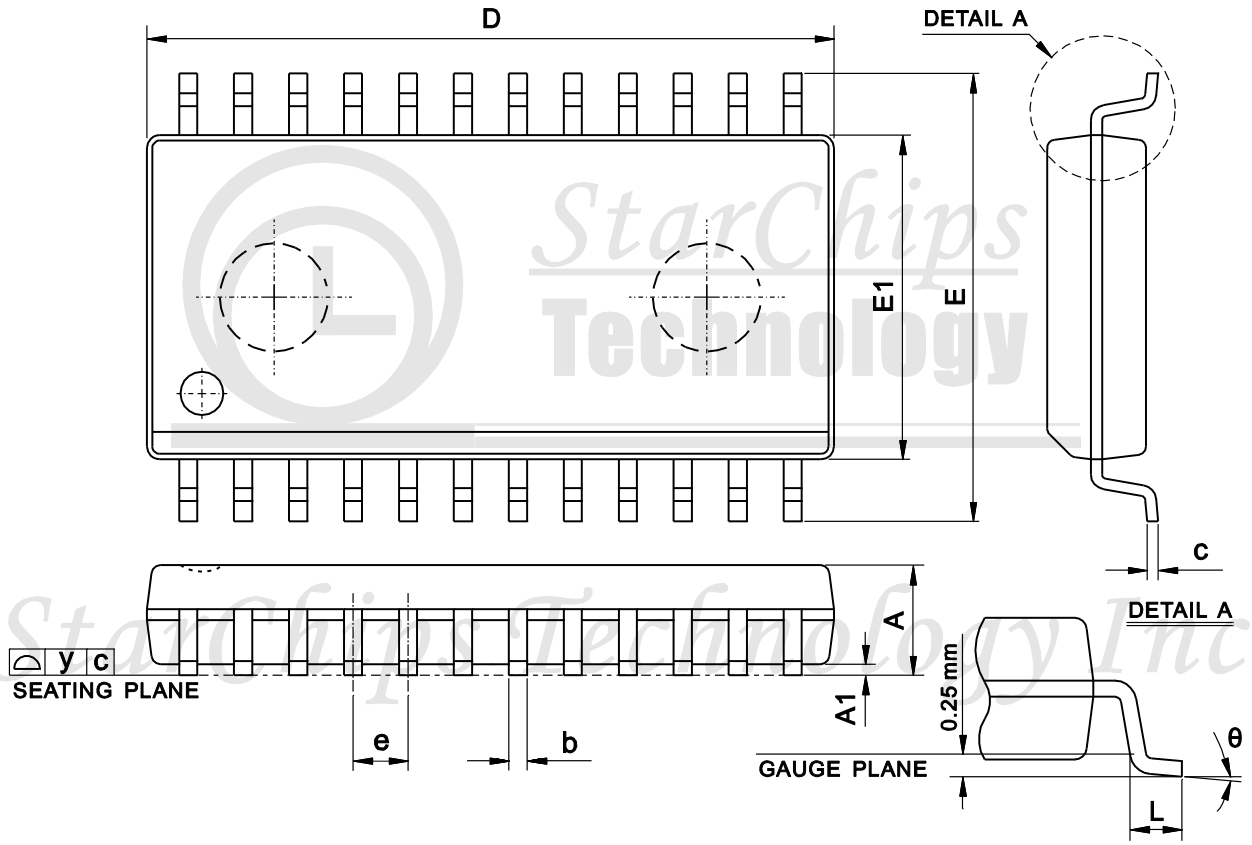
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.63	1.75	53.1	64.2	68.9
A1	0.10	0.15	0.25	3.9	5.9	9.8
A2	-	-	1.50	-	-	59.1
b	0.20	-	0.30	7.9	-	11.8
c	0.18	-	0.25	7.1	-	9.8
D	8.56	8.66	8.74	337.0	340.9	344.1
E	5.79	5.99	6.20	228.0	235.8	244.1
E1	3.81	3.91	3.99	150.0	153.9	157.1
e	0.64 BSC			25.0 BSC		
L	0.41	0.64	1.27	16.1	25.0	50.0
y	-	-	0.10	-	-	3.9
ZD	0.84 REF			33.0 REF		
θ	0°	-	8°	0°	-	8°

SSOP24-1 (check up-to-date version)



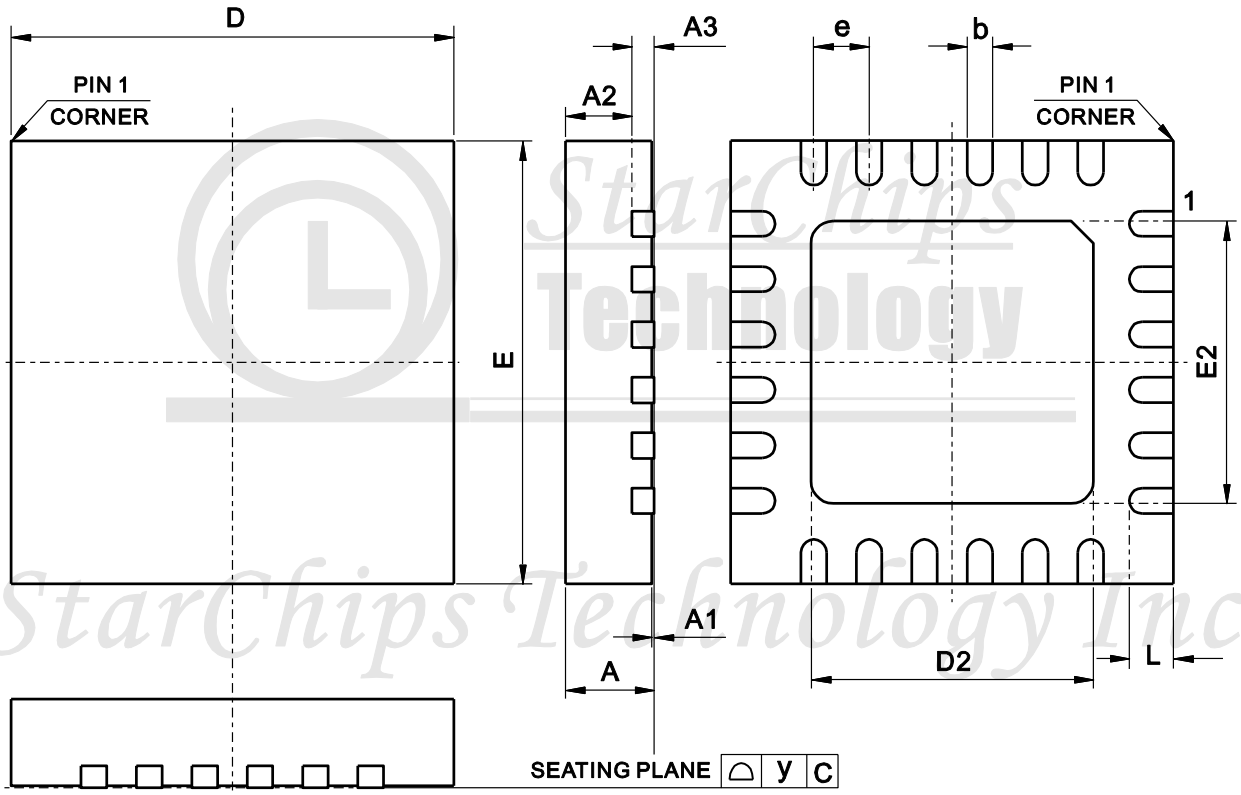
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.90	-	-	74.8
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.30	1.50	1.70	51.2	59.1	66.9
b	0.30	0.40	0.52	11.8	15.7	20.5
c	0.10	0.15	0.27	3.9	5.9	10.6
D	12.80	13.00	13.20	503.9	511.8	519.7
E	7.70	8.00	8.30	303.1	315.0	326.8
E1	5.80	6.00	6.20	228.3	236.2	244.1
e		1.00 BSC			39.4 BSC	
L	0.25	0.45	0.65	9.8	17.7	25.6
y	-	-	0.10	-	-	3.9
θ	0°	-	10°	0°	-	10°

SOP24 (check up-to-date version)



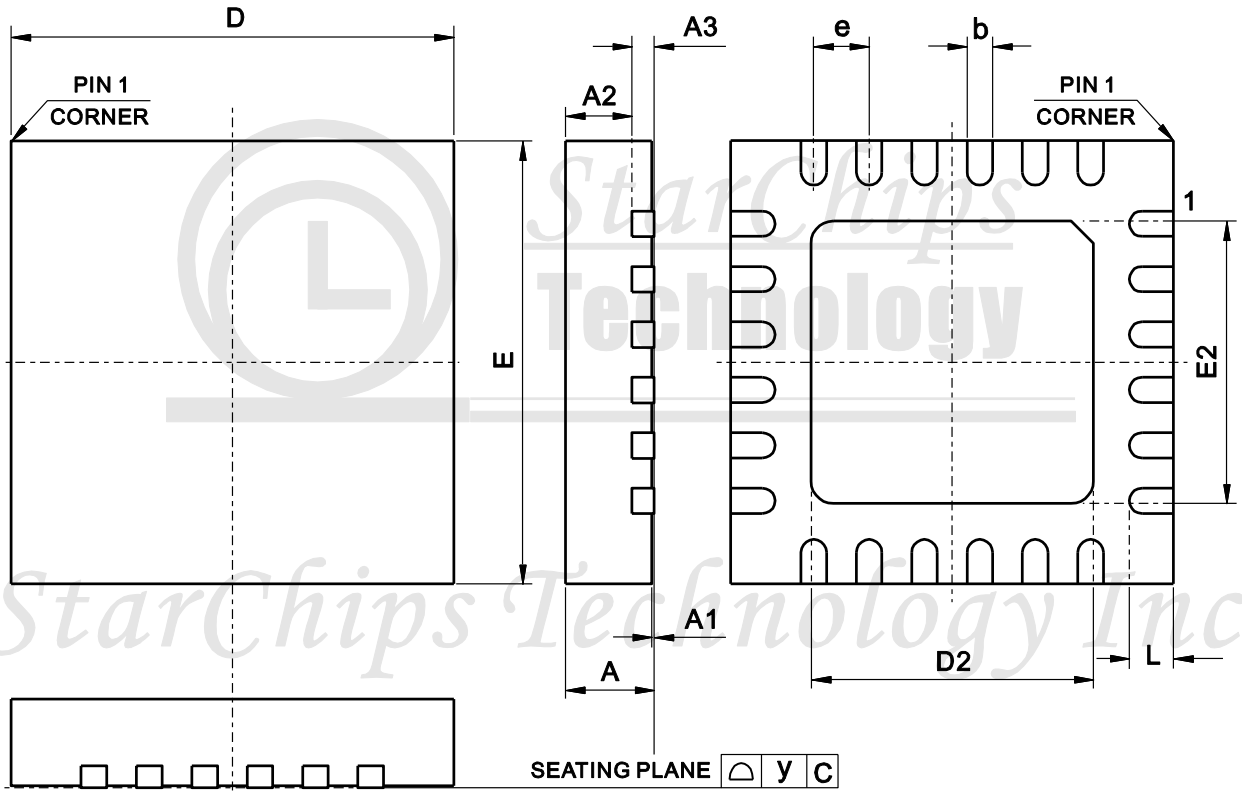
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.35	-	2.65	92.5	-	104.3
A1	0.10	-	0.30	3.9	-	11.8
b	0.33	-	0.51	13.0	-	20.1
c	0.23	-	0.32	9.1	-	12.6
D	15.20	-	15.60	598.4	-	614.2
E	10.00	-	10.65	393.7	-	419.3
E1	7.40	-	7.60	291.3	-	299.2
e	1.27 BSC			50.0 BSC		
L	0.40	-	1.27	15.7	-	50.0
θ	0°	-	8°	0°	-	8°
y	-	-	0.10	-	-	3.9

TQFN24-4x4(CQNG) (check up-to-date version)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.76	0.80	0.84	30.0	31.0	33.0
A1	0.00	0.02	0.04	0.0	0.8	1.5
A2	0.57	0.60	0.63	22.0	24.0	25.0
A3		0.20 REF			8.0 REF	
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	154.0	157.0	161.0
D2	2.50	2.55	2.60	98.4	100.4	102.4
E	3.90	4.00	4.10	154.0	157.0	161.0
E2	2.50	2.55	2.60	98.4	100.4	102.4
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y	-	0.08	-	-	3.1	-

TQFN24-4x4(AQNG) (check up-to-date version)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0.00	0.035	0.05	0.0	1.4	2.0
A2	-	0.55	0.57	-	21.7	22.4
A3		0.203 REF			8.0 REF	
b	0.20	0.25	0.30	7.9	9.8	11.8
D		4.00 BSC			157.0 BSC	
D2	2.40	2.50	2.60	94.5	98.4	102.4
E		4.00 BSC			157.0 BSC	
E2	2.40	2.50	2.60	94.5	98.4	102.4
e		0.50 BSC			19.7 BSC	
L	0.35	0.40	0.45	13.8	15.7	17.7
y	-	0.08	-	-	3.1	-

Revision History(check up-to-date version)

Data Sheet Version	Remark
V01_01	First released

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