High-Speed CAN Transceiver With Standby Mode

1. Description

The TJA1042 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

Table 1. Quick Reference Data

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	V_{CC}		4.5	5.5	V
Maximum transmission rate	$1/t_{bit}$	Non-return to zero code	5		Mbaud
CANH/CANL input or output voltage	V_{can}		-70	+70	V
Bus differential voltage	V_{diff}		1.5	3.0	V
Virtual junction temperature	T_{vj}		-40	150	°C

2. Features

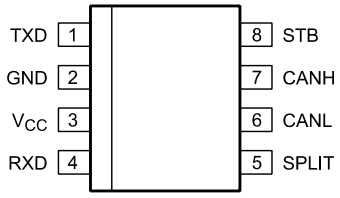
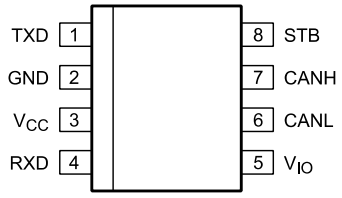
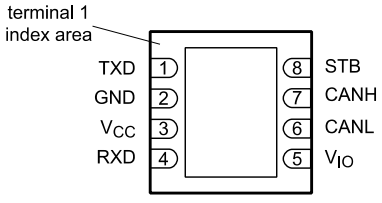
- Fully compatible with the ISO 11898 standard
- Thermally protected
- Transmit Data (TXD) dominant time-out function
- Very low-current Standby mode with host and bus wake-up capability
- V_{IO} input on TJA1042T/3 and TJA1042TK/3 allows for direct interfacing with 3 V to 5 V microcontrollers
- Transmit Data (TXD) dominant time-out function
- High voltage robustness on CAN pins (±70 V)
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Undervoltage detection on pins V_{CC} and V_{IO}
- Bus-dominant time-out function in Standby mode

3. Ordering Information

Type Number	Package Type	Packing	Notes
TJA1042T	SOIC-8	Tape & Reel	
TJA1042T/3	SOIC-8	Tape & Reel	
TJA1042TK/3	DFN3*3-8/HVSON8	Tape & Reel	

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

4. Pin Configuration

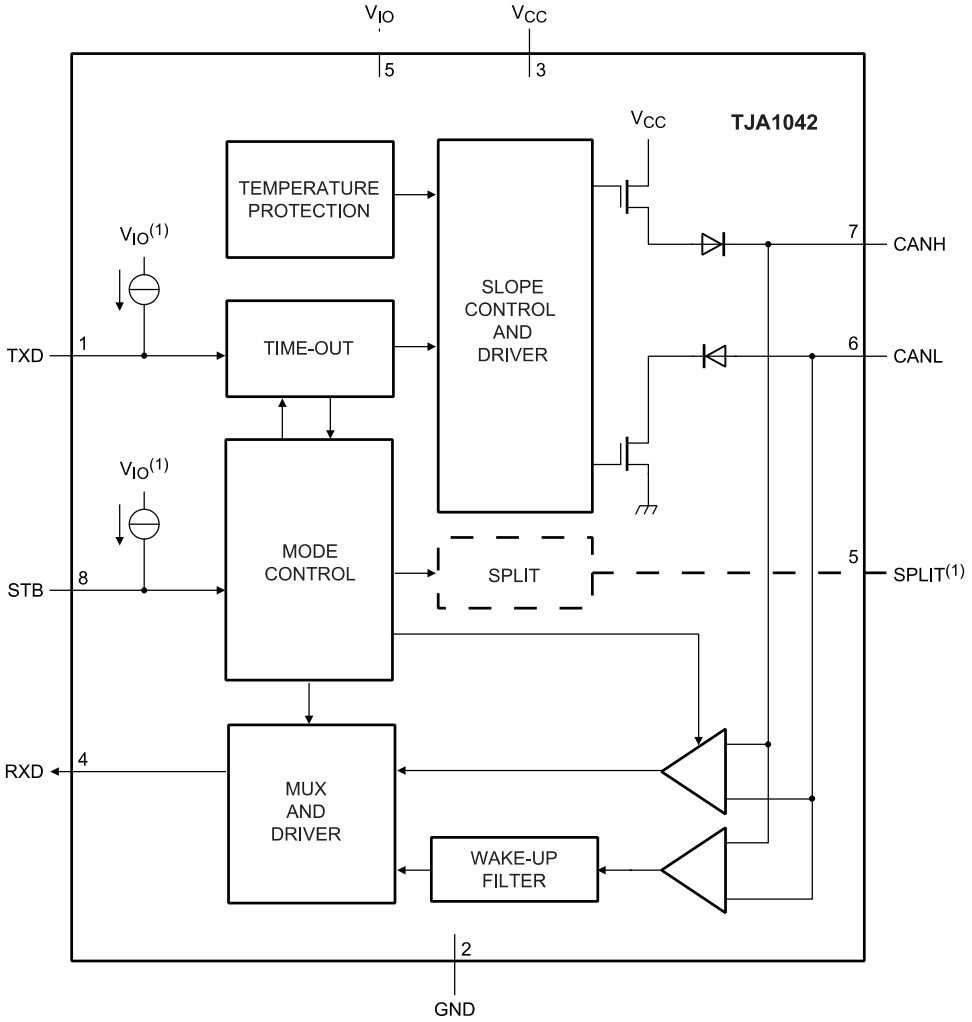
TJA1042T SOIC-8	TJA1042T/3 SOIC-8	TJA1042TK/3 DFN3*3-8
		

5. Pin Description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
SPLIT	5	common-mode stabilization output; in TJA1042T version only
V_{IO}	5	supply voltage for I/O level adapter; in TJA1042T/3 and TJA1042TK/3 versions only
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
STB	8	Standby mode control input

[1]: HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

6. Functional Block Diagram



(1) In a transceiver with a SPLIT pin, the V_{IO} input is internally connected to V_{CC}.

7. Limiting Values

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	V_{CC}	-0.3~+7	V
Voltage on MCU pins	TXD，RXD，STB，V_{IO}	-0.3~+7	V
Voltage range at any bus terminal (CANH, CANL)	CANL，CANH	-70~70	V
Voltage between pin CANH and pin CANL	$V_{CANH-CANL}$	-27~27	V
Transient voltage on pins CANH, CANL and SPLIT	V_{tr}	-200~+200	V
Storage temperature		-55~150	℃
Virtual junction temperature	T_{vj}	-40~150	℃
Welding temperature range		300	℃

The maximum limit parameters means that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal opration of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

8. Driver Electrical Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	V_I=0V, STB=0V, R_L=60Ω, Fig.1, Fig.2	2.9	3.4	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.8		1.5	V
Bus recessive output voltage	$V_{O(R)}$	V_I=3V, STB=0V, R_L=60Ω, Fig.1, Fig.2	2	0.5V_{CC}	3	V
Bus dominant differential output voltage	$V_{OD(D)}$	V_I=0V, STB=0V, R_L=60Ω, Fig.1, Fig.2	1.5		3	V
Bus recessive differential output voltage	$V_{OD(R)}$	V_I=3V, S=0V, Fig.1, Fig.2	-0.012		0.012	V
		V_I=3V, STB=0V, NO LOAD	-0.5		0.05	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}$ = V_{CC}- V_{CANH} - V_{CANL}	-400		400	mV
Transmitter voltage symmetry	V_{TXsym}	V_{TXsym} = V_{CANH} + V_{CANL}	0.9V_{CC}		1.1V_{CC}	V
Common-mode output voltage	V_{OC}	STB=0V, Fig.8	2	0.5V_{CC}	3	V
Peak-to-peak Common-mode output voltage	ΔV_{OC}			30		mV
Short-circuit output current	I_{OS}	CANH=-12V, CANL=open, Fig.11	-105	-72		mA
		CANH=12V, CANL=open, Fig.11		0.36	1	mA
		CANL=-12V, CANH=open, Fig.11	-1	0.5		mA
		CANL=12V, CANH=open, Fig.11		71	105	mA
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0<V_{CC}<5.25V	-2.0		2.5	mA

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

9. Driver Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	STB=0V, Fig.4		90		ns
Propagation delay time, low-to-high-level output	t_{PHL}			65		ns
Differential output signal rise time	t_r			45		ns
Differential output signal fall time	t_f			45		ns
Enable time from standby mode to dominant	t_{EN}	Fig.7		10	45	μs
TXD dominant time-out time	t_{dom_TXD}	Fig 10	0.8	2	4	ms
Bus dominant time-out time	t_{dom_BUS}		0.8	2	4	ms
Bus wake-up filter time	t_{WAKE}		0.5		5	μs

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

10. Receiver Electrical Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	V_{IT+}	STB=0V, Fig.5			900	mV
Negative-going input threshold voltage	V_{IT-}		500			mV
Hysteresis voltage (V_{IT+} – V_{IT-})	V_{HYS}		50	120	200	mV
Positive-standby input threshold voltage	$V_{IT+(STB)}$	Standby mode			1150	mV
Negative-standby input threshold voltage	$V_{IT-(STB)}$	Standby mode	400			mV
Power-off bus input current	$I_{(OFF)}$	CANH or CANL=5V, Other pin=0V	-5		5	μA
Input capacitance to ground, (CANH or CANL)	C_I			24		pF
Differential input capacitance	C_{ID}			12		pF
Input resistance,(CANH or CANL)	R_{IN}	TXD=V_{IO}, STB=0V	9	15	28	kΩ
Differential input resistance	R_{ID}		19	30	52	kΩ
Input resistance matching	R_{Imatch}	CANH=CANL	-2%		2%	
The range of common-mode voltage	V_{COM}		-30		30	V

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

11. Receiver Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	STB=0V or V_{CC}, Fig.6		65		ns
Propagation delay time, low-to-high-level output	t_{PHL}			60		ns
RXD signal rise time	t_r			10		ns
RXD signal fall time	t_f			10		ns

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

12. Device Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay1, driver input to receiver output, Recessive to Dominant	$T_{d(LOOP1)}$	STB=0V, Fig.9		90	220	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	$T_{d(LOOP2)}$			100	220	ns
Bit time on Bus	$t_{bit(BUS)}$	$t_{bit(TXD)}$=500ns	435		530	ns
		$t_{bit(TXD)}$=200ns	155		210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$=500ns	400		550	ns
		$t_{bit(TXD)}$=200ns	120		220	ns

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

13. Over Temperature Protection

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			190		°C

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

14. Undervoltege Detection

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
undervoltage detection voltage on pin V_{CC}	V_{uvd_VCC}		3.5		4.5	V
undervoltage detection voltage on pin V_{IO}	V_{uvd_VIO}		1.5		2.5	V

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

15. TXD-Pin Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{IH(TXD)}$	TXD=V_{IO}	-5		5	μA
LOW-level input current	$I_{IL(TXD)}$	TXD=0V	-260	-150	-30	μA
When V_{CC}=0V, current on TXD pin	$I_{O(OFF)}$	V_{CC}=V_{IO}=0V, TXD=V_{IO}	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7V_{IO}①		V_{IO}①+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.3V_{IO}①	V
Open voltage on TXD pin	T_{XDO}		H			logic

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

16. STB Pin Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current on STB Pin	$I_{IH(STB)}$	STB=V_{IO}	-2		2	μA
LOW-level input current on STB Pin	$I_{IL(STB)}$	STB=0V	-20		-2	μA
V_{CC}=0V, STB Pin current	I_O(off)	V_{CC}=V_{IO}=0V, STB=V_{IO}	-1		1	μA
HIGH-level input voltage	V_{IH}		0.7 V_{IO}①		V_{IO}①+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.3V_{IO}①	V
Open voltage on STB Pin	STB_O		H			logic

①TJA1042T, V_{IO}=V_{CC} (Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

17. RXD Pin Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{OH(RXD)}$	$V_{IO}=V_{CC}$, RXD=V_{IO}-0.4V	-8	-3	-1	mA
LOW-level input current	$I_{OL(RXD)}$	RXD=0.4V, BUS dominat	2	5	12	mA
When V_{CC}=0V, current on STB pin	$I_{O(off)}$	$V_{CC}=V_{IO}$=0V, RXD=V_{IO}	-1		1	μA

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

18. Common Mode Stabilization Output

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SPLIT Pin output voltage	V_{SPLIT}	-500μA<I_{SPLIT}<500μA	0.3V_{CC}	0.5 V_{CC}	0.7V_{CC}	V

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

19. Supply Current

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply current on Pin V_{CC}	Common Mode Dominant	I_{CC_D}	Bus dominant		45	70	mA
	Common Mode Recessive	I_{CC_R}	Bus recessive		5	10	mA
	Standby Mode	I_{CC_STB}	STB=V_{CC}, TXD=V_{IO}, (TJA1042T/3)		0.5	5	μA
			STB=V_{CC}, TXD=V_{CC}, (TJA1042T)		12	25	μA
Supply current on Pin V_{IO}	Common Mode Dominant	I_{IO_D}	RXD open, STB=0V, TXD=0V		350	1000	μA
	Common Mode recessive	I_{IO_R}	RXD open, STB=0V, TXD=V_{IO}		80	200	μA
	Standby Mode	I_{IO_STB}	STB=TXD=V_{IO}		10	20	μA

(Typical in V_{CC}=+5V, V_{IO}=5V, R_L=60Ω and T_{emp}=25°C unless specified otherwise)

20. ESD Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
At any other pin (IEC)	V_{ESD_IEC}	IEC 61000-4-2: Contact Discharge (CANH，CANL)	-4		+4	kV
Human Body Model (HBM)	V_{ESD_HBM}		-8		+8	kV
Charged Device Model (CDM)	V_{CDM}		-750		+750	V
Machine Model (MM)	V_{MM}		-300		+300	V

21. Function Table

Table 2. CAN Transceiver Truth Table

TXD(1)	STB(1)	CANH(1)	CANL(1)	BUS State	RXD(1)
L	L	H	L	Domiant	L
H or Open	L	$0.5V_{CC}$	$0.5V_{CC}$	Recessive	H
X	H or Open	GND	GND	Recessive	H

(1) H=high level; L=low level; X=irrelevant

Table 3. Receiver Function Table

V_{ID}=CANH-CANL	RXD(1)	Bus State(1)
V_{ID}≥0.9V	L	Dominate
0.5< V_{ID}<0.9V	?	?
V_{ID}≤0.5V	H	Recessive
Open	H	Recessive

(1) H=high-level; L=low-level; ?=uncertain

Table 4. Under-voltage protection status table

V_{CC}	V_{IO}(1)	BUS State	BUS Output(2)	RXD(2)
V_{CC} > V_{uvd_VCC}	V_{IO} > V_{uvd_VIO}	normal	According to STB and TXD	Follow Bus
V_{CC} < V_{uvd_VCC}	V_{IO} > V_{uvd_VIO}	Protected state	GND	H
V_{CC} > V_{uvd_VCC}	V_{IO} < V_{uvd_VIO}	Protected state	Z	H
V_{CC} < V_{uvd_VCC}	V_{IO} < V_{uvd_VIO}	Protected state	Z	H

1 Only TJA1042T/3

2 H=High Level；Z=High impedance;

22. Additional Description

Operating Modes

Mode	Pin STB	Pin RXD	
		LOW	HIGH
Common	LOW	bus dominant	bus recessive
Standby	HIGH	wake-up request detected	no wake-up request detected

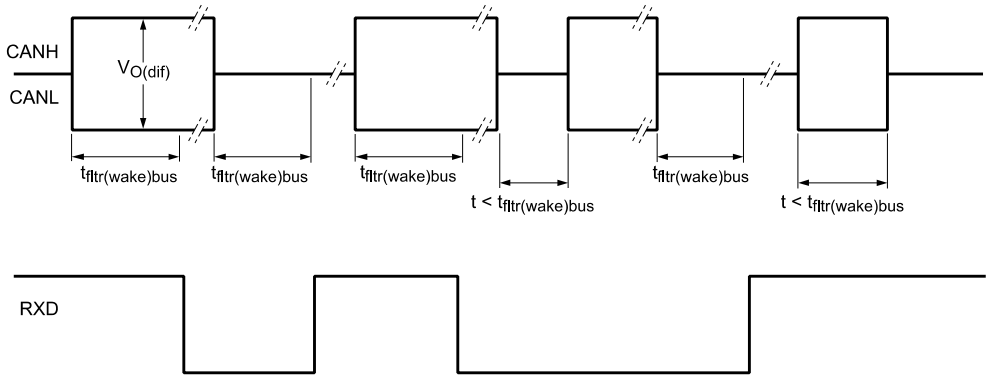
Common Mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

Standby Mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.



Current protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Over temperature protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature becomes lower than $T_{j(sd)}$ and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} drop below the V_{CC} undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until V_{CC} has recovered.

Should V_{IO} drop below the V_{IO} undervoltage detection level, $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

23. Test Circuit

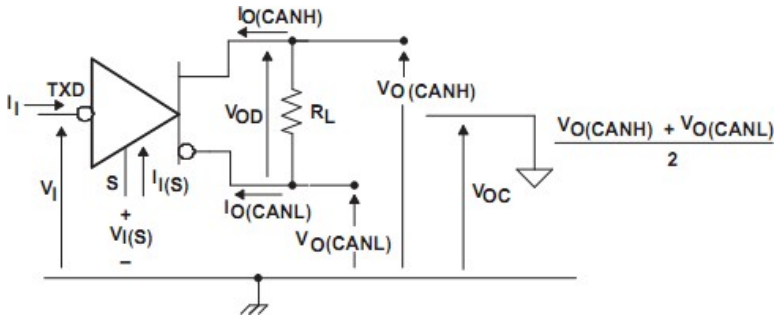


Fig. 1. Driver Voltage, Current, and Test Definition

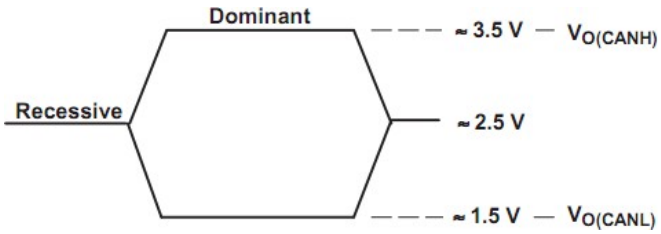


Fig. 2. Bus Logic State Voltage Definition

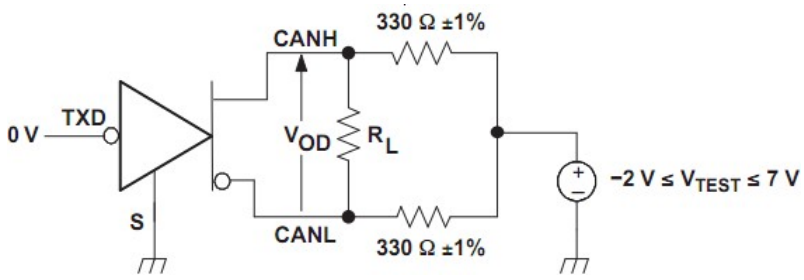


Fig. 3. Driver VOD Test Circuit

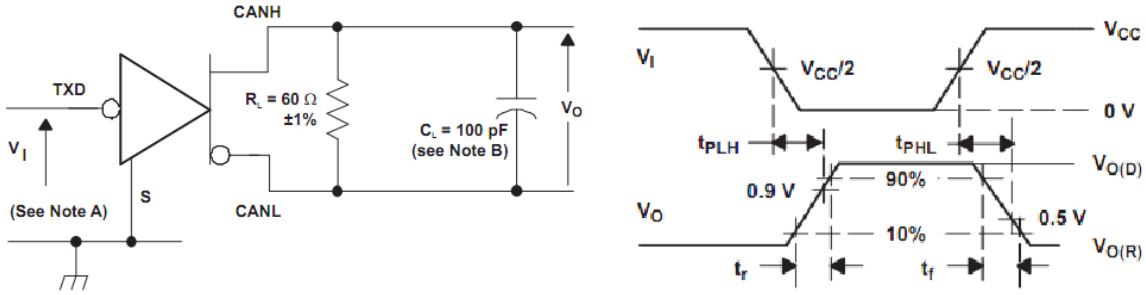


Fig. 4. Driver Test Circuit and Waveform

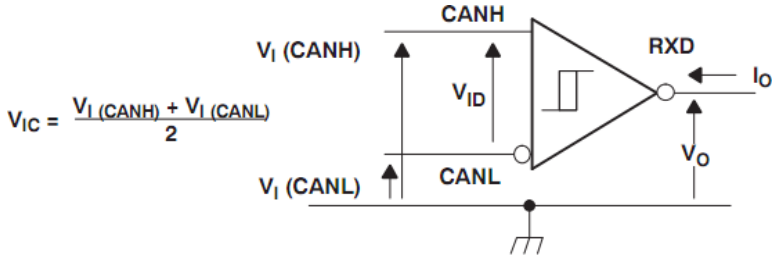
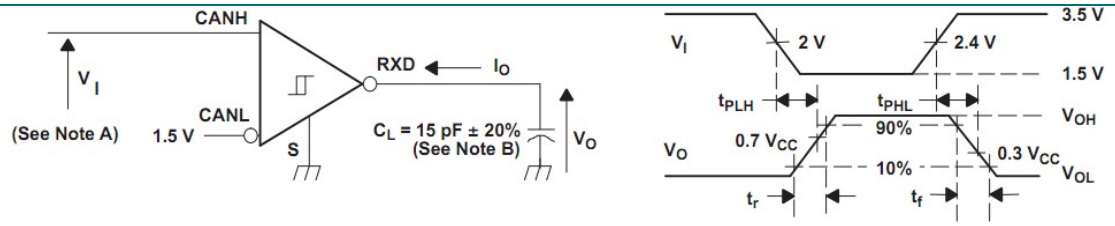


Fig. 5. Receiver Voltage and Current Definition



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, tr ⩽ 6 ns, tf ⩽ 6ns, ZO = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Fig. 6. Receiver Test Circuit and Waveform

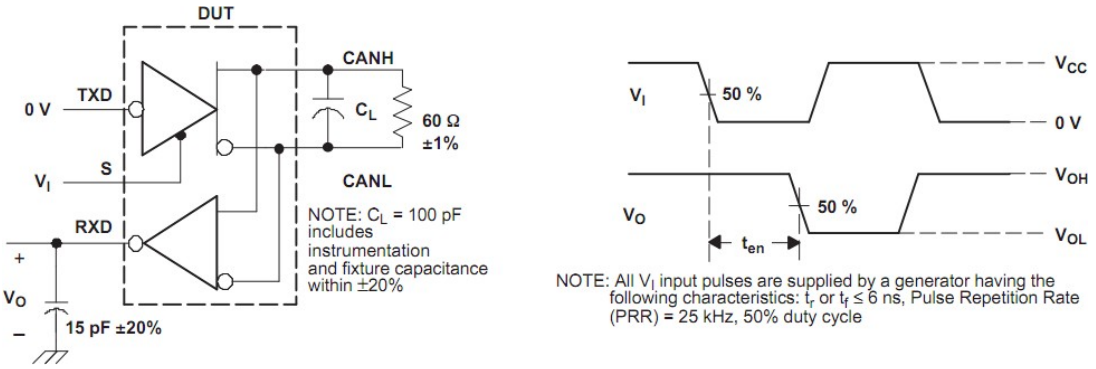
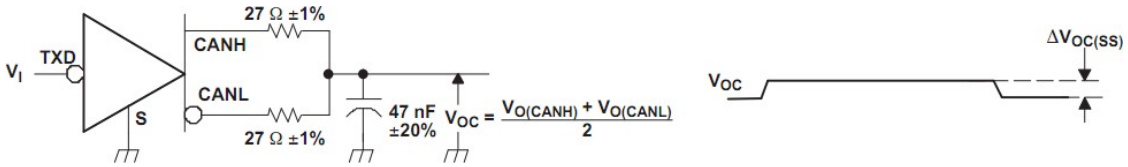


Fig. 7. t_{EN} Test Circuit and Waveform



All VI input pulses are from 0 V to VCC and supplied by a generator having the following characteristics: tr or tf ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Fig. 8. Peak-to-Peak Common Mode Output Voltage Test and Waveform

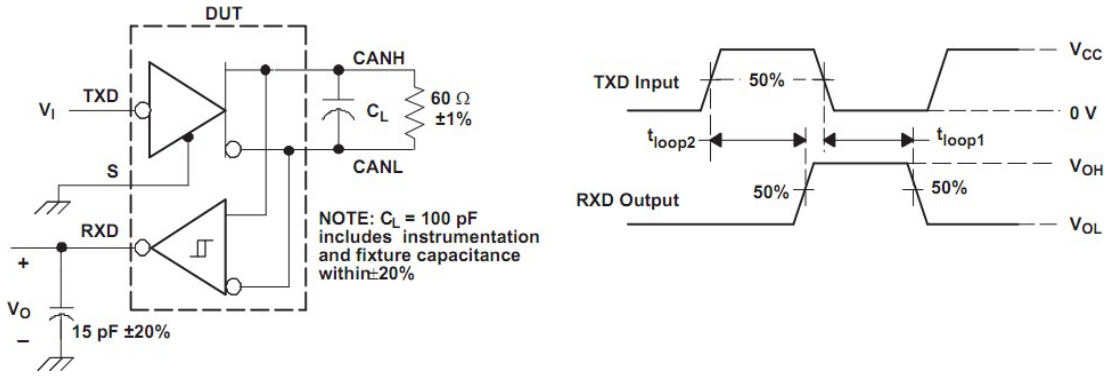


Fig. 9. $t_{(LOOP)}$ Test Circuit and Waveform

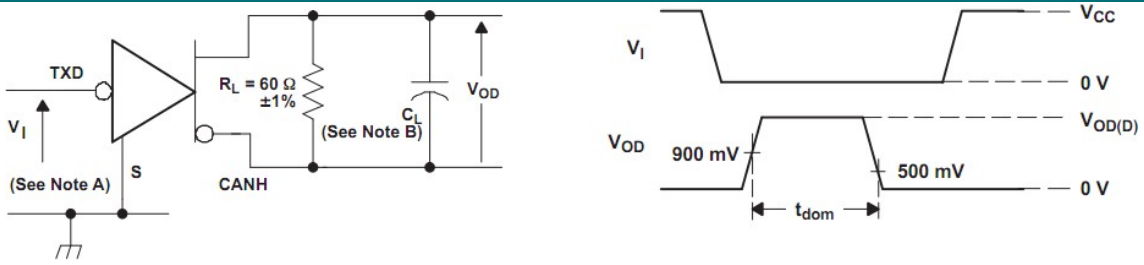


Fig. 10. Dominant Time-Out Test Circuit and Waveform

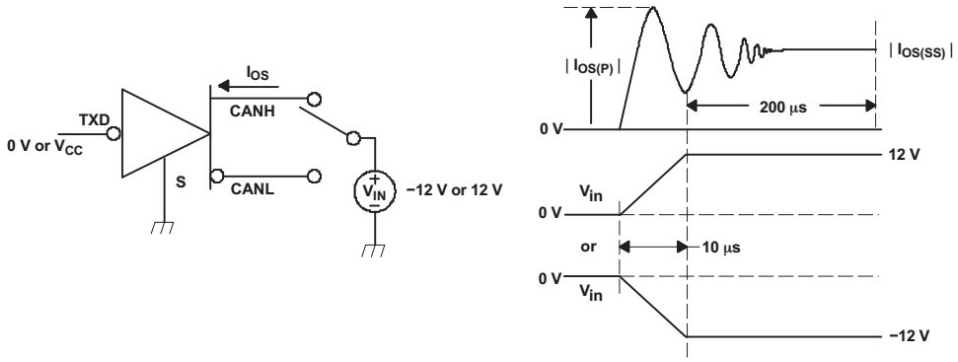


Fig. 11. Driver Short-Circuit Current Test Circuit and Waveform

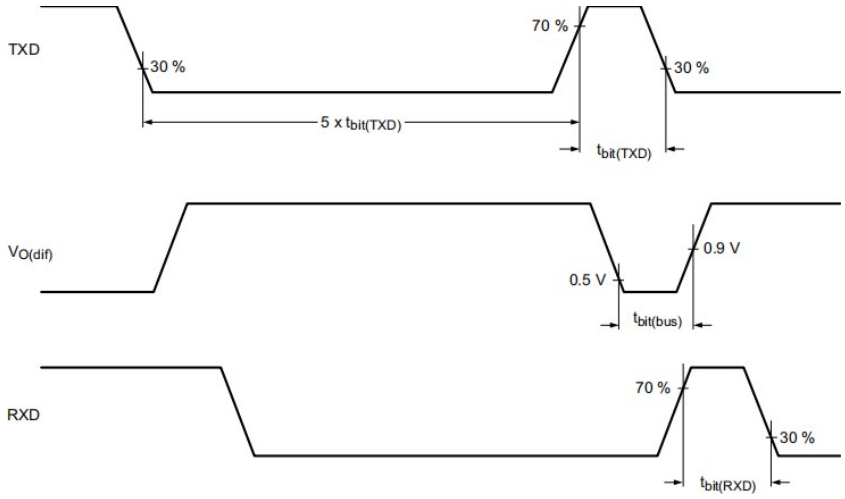
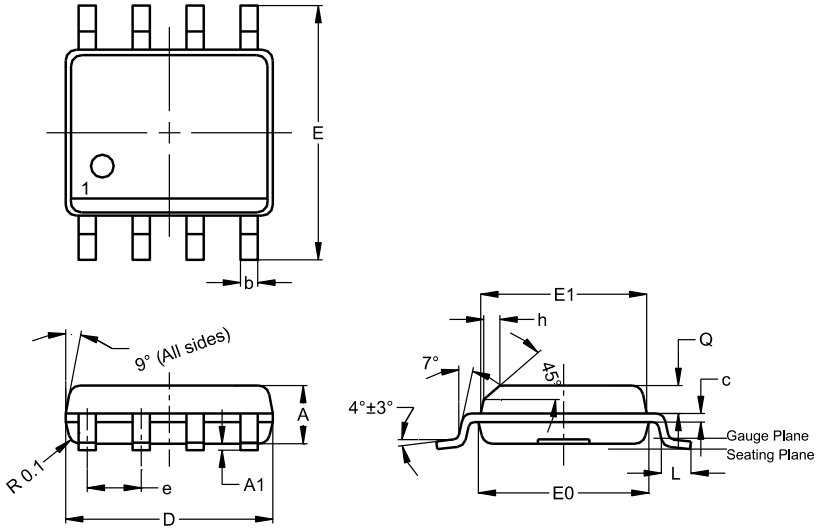


Fig. 12. $t_{bit(RXD)}$ Test Circuit and Waveform

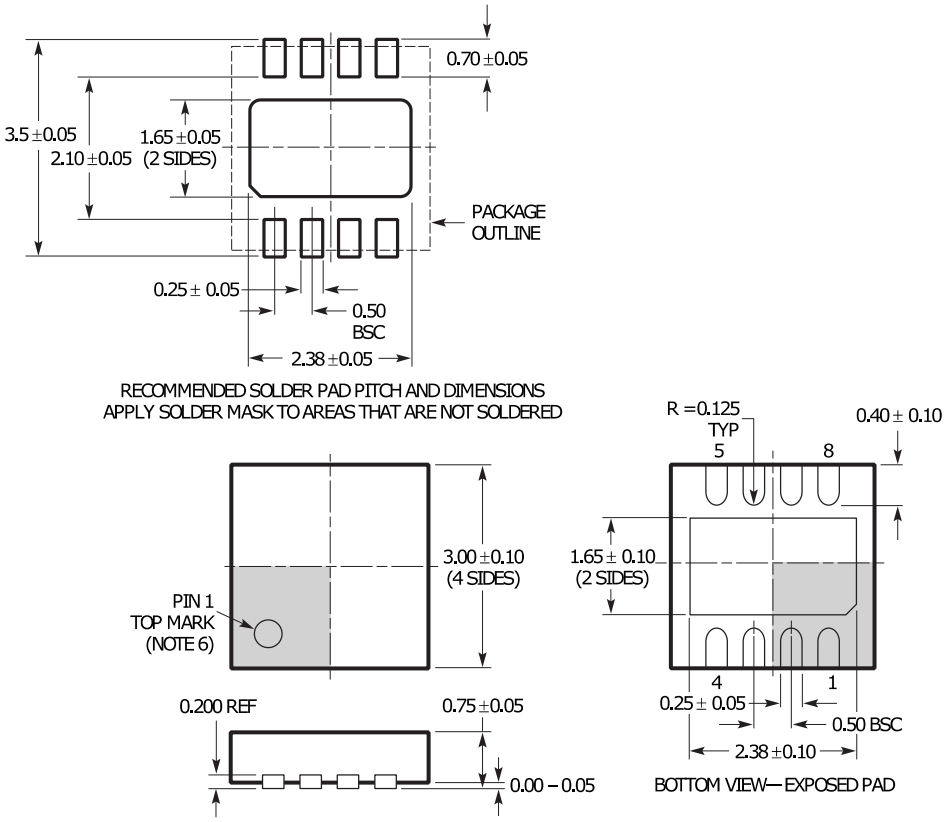
24. Package Outlines

SOIC-8



SOIC-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

DFN3*3-8



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